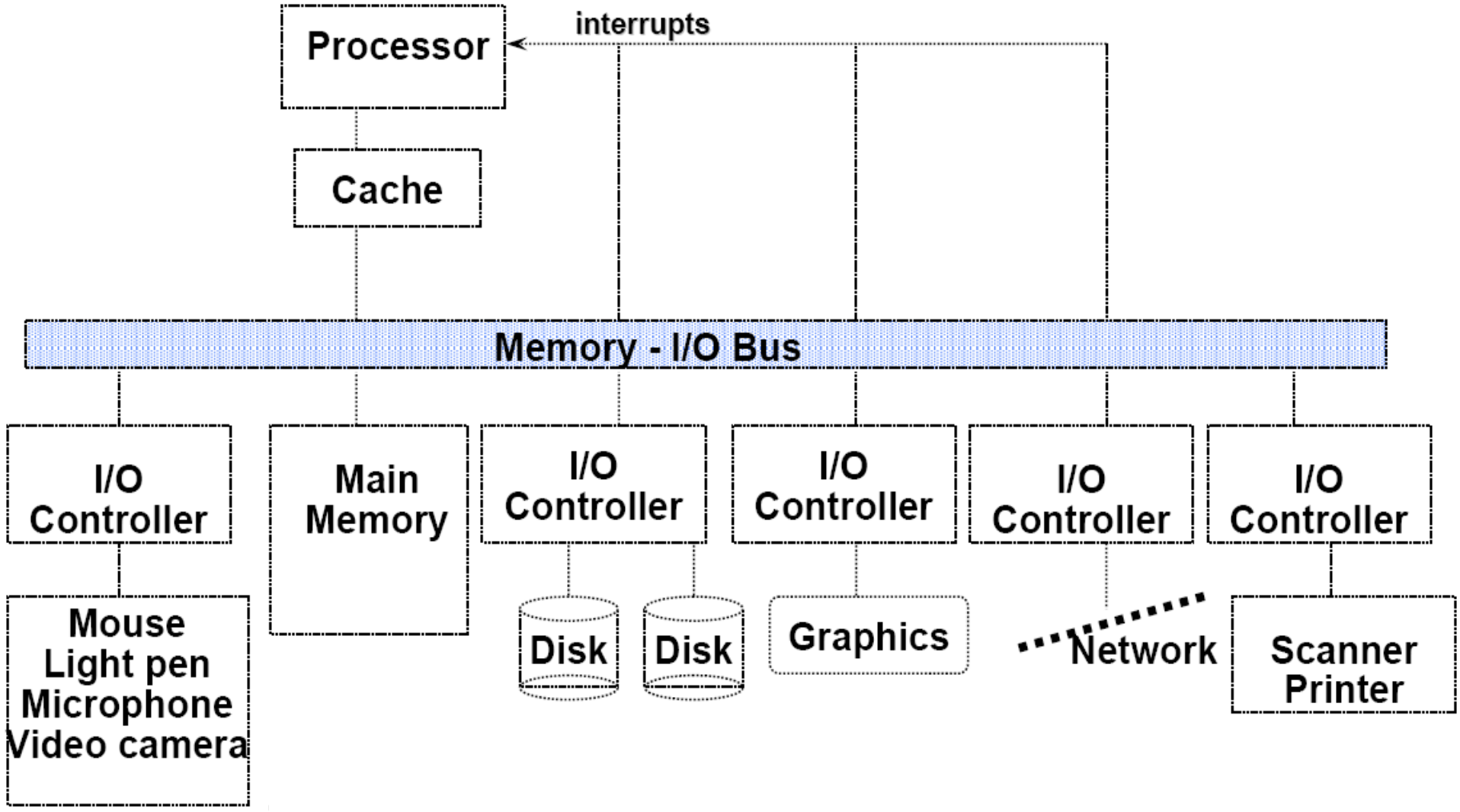
C9 PC BUSES

Outline:

1. **INTRODUCTION**
2. **ISA Bus**
3. **ISA Bus signals**
4. **ISA Interface Design**

I/O Systems


Processor
interrupts
Cache
Memory - I/O Bus
I/O Controller
Main Memory
I/O Controller
I/O Controller
I/O Controller
I/O Controller
Mouse
Light pen
Microphone
Video camera
Disk
Disk
Graphics
Network
Scanner
Printer

1. INTRODUCTION

BUS - represents a set of lines (wires) on which the information is passed between two or more devices

µP BUS types: Address, Data, Control

Buses features:

- **Bus width:** refers usually to the data part. If the bus is large, more information may be transferred on it, having a better performance;
- **Speed**: indicates the binary flow on each bus line. Most of the buses are transmitting 1bit/line/cycle, but the new buses like AGP can transmit 2bits/line/cycle, thus doubling the performances;
- **Band (rate) of the bus:** indicates the quantity of data that can be transferred theoretically by the bus in a given unit of time

!!! Considering that *the processor is the fastest device* in a modern computer, the buses can be classified using the distance between them and the processor, the greater the distance is the slower the bus is:

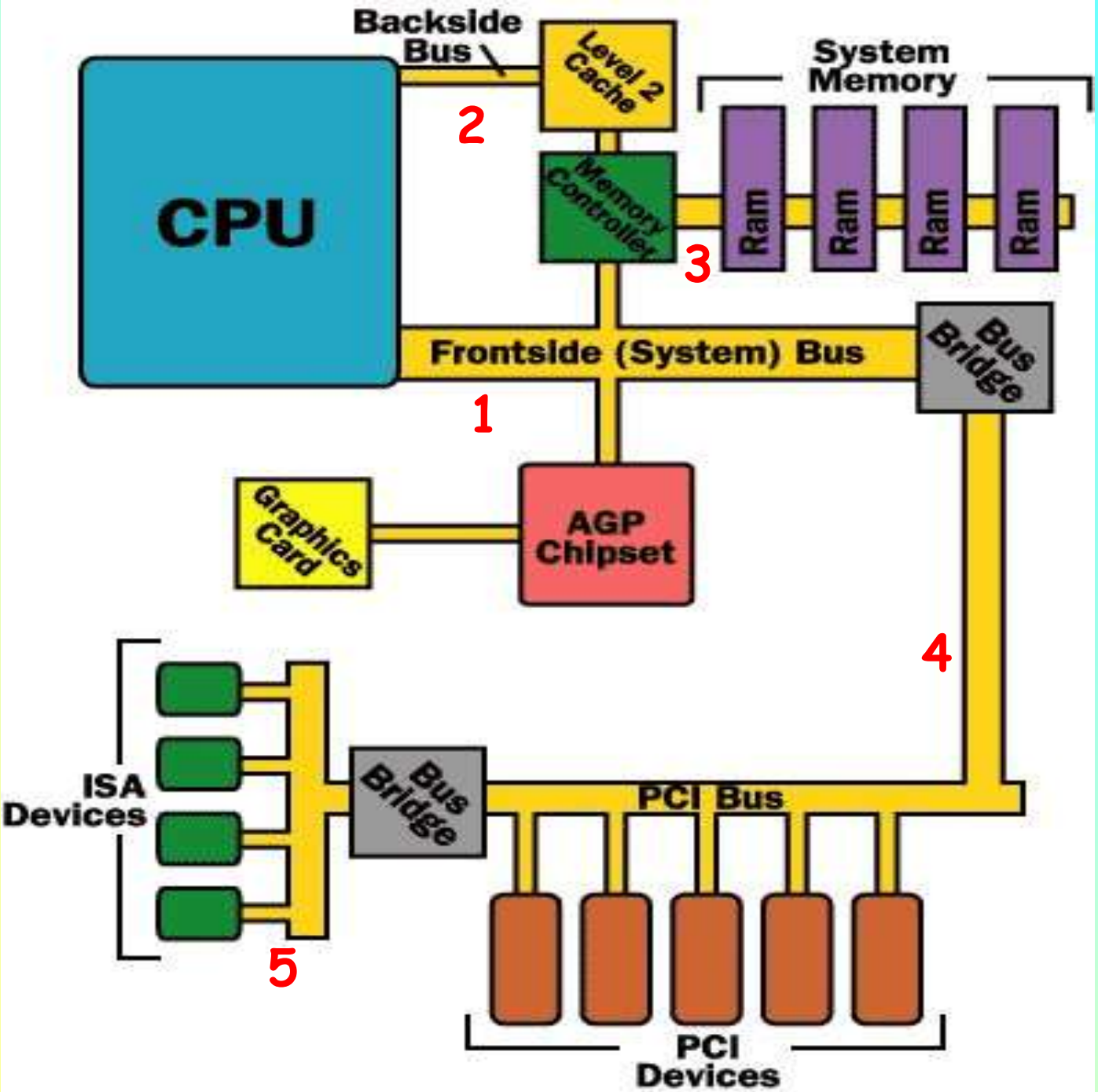
- **Processor bus** – represents the bus with the higher level, used by the chip-set to exchange information with the processor;

- **Cache bus** – introduced in recent architectures (used in Pentium Pro and Pentium II), being dedicated to system cache memory access. It is sometimes called **"backside bus".** Main boards from the 5-th generation used by conventional processors have the cache memory connected to the standard memory bus;

- **Memory bus** – is a level 2 bus, which connects the memory to the chip-set and processor. In some systems, the memory bus and the processor bus are one and the same;

- **Local I/O bus** – is a high speed I/O bus used to connect the peripheral devices to the memory, to the processor and to the system chip-set. The used I/O buses of this type are: VLBus (Video Local Bus or VESA) and PCI (Peripheral Component Interconnect) bus, PCIx;

- **Standard I/O bus** – is the oldest I/O bus used by slow peripheral devices (mouse, modem, sound cards, slow network cards). This is the ISA bus (Industry Standard Architecture) or AT bus.


Backside Bus
Level 2 Cache
System Memory
CPU
2
Memory Controller
Ram
Ram
Ram
Ram
3
Frontside (System) Bus
Bus Bridge
1
Graphics Card
AGP Chipset
4
ISA Devices
Bus Bridge
PCI Bus
5
PCI Devices
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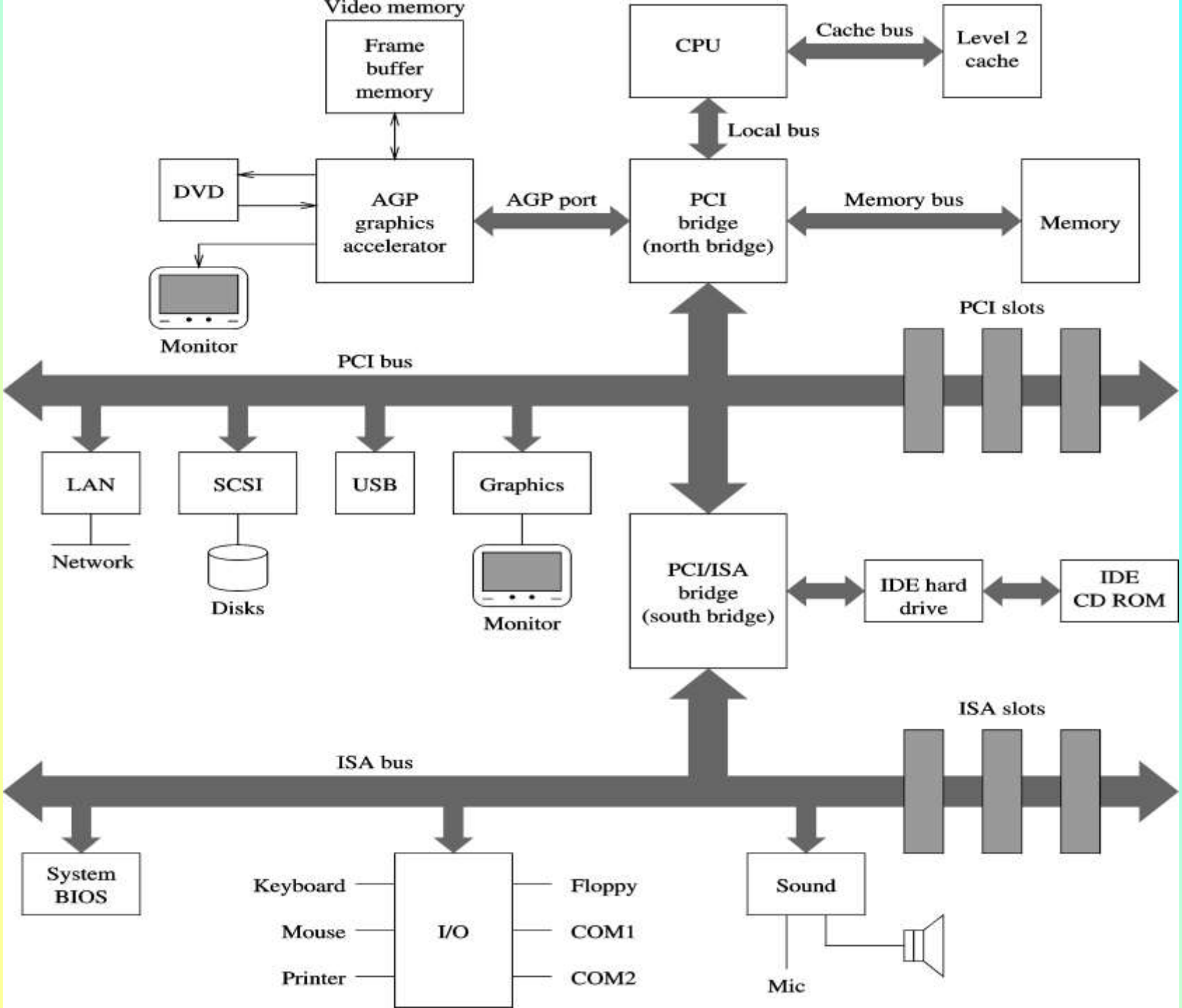
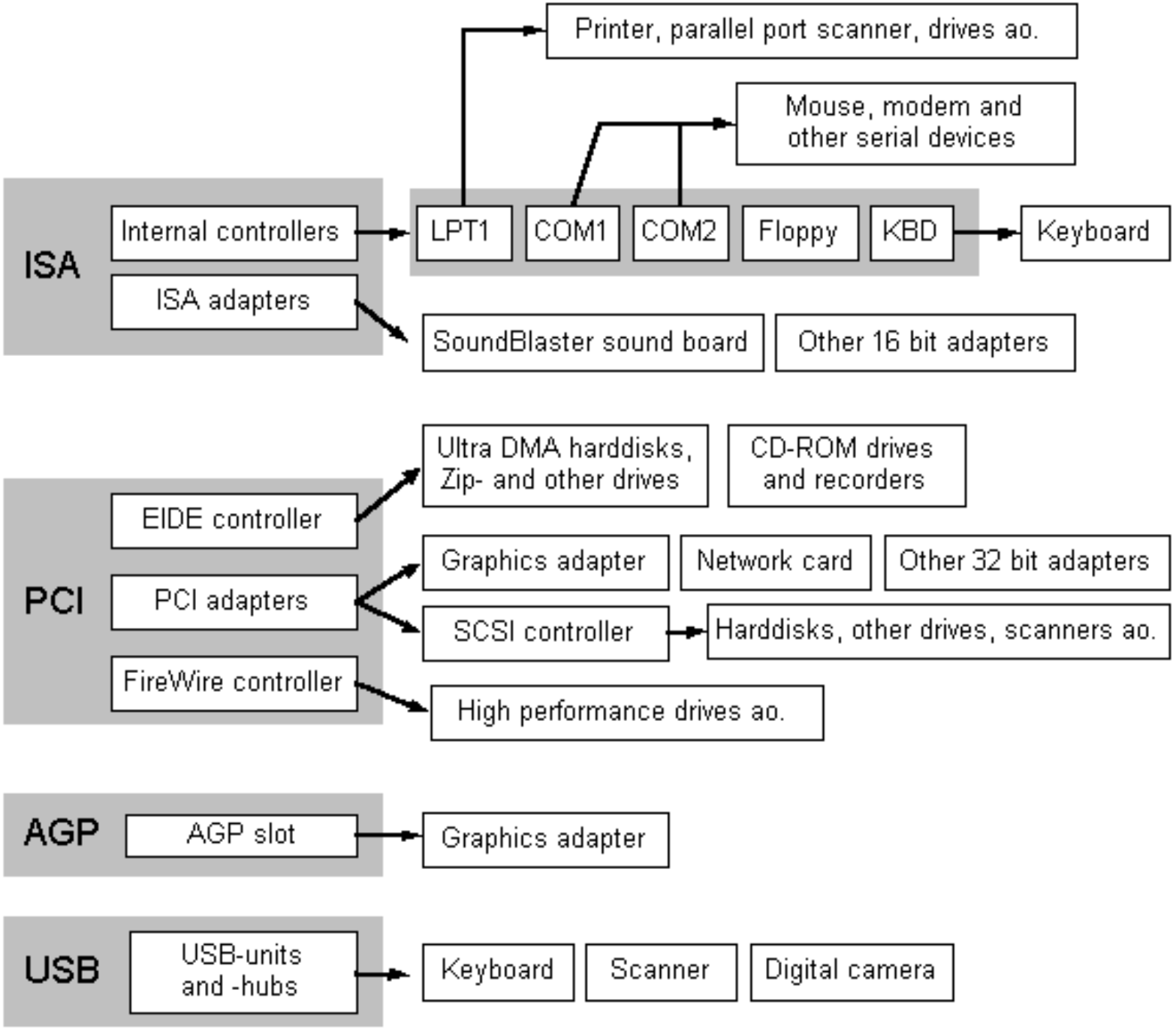
Bus	Width (bit)	Bandwidth (MB/s)
16-bit ISA	16	15.9
EISA	32	31.8
VLB	32	127.2
PCI	32	127.2
64-bit PCI 2.1 (66 MHz)	64	508.6
AGP 8x	32	2,133
USB 2	1	Slow-Speed: 1.5 Mbit/s Full-Speed: 12 Mbit/s Hi-Speed: 480 Mbit/s
Firewire 400	1	400 Mbit/s
PCI-Express 16x version 2	16	8,000

I/O Buses Performances (Theoretical)


Video memory
Frame buffer memory
CPU
Cache bus
Level 2 cache
Local bus
DVD
AGP graphics accelerator
AGP port
PCI bridge (north bridge)
Memory bus
Memory
Monitor
PCI slots
PCI bus
LAN
SCSI
USB
Graphics
Network
Disks
Monitor
PCI/ISA bridge (south bridge)
IDE hard drive
IDE CD ROM
ISA slots
ISA bus
System BIOS
Keyboard
Mouse
Printer
I/O
Floppy
COM1
COM2
Sound
Mic


Printer, parallel port scanner, drives ao.
Mouse, modem and other serial devices
ISA
Internal controllers
ISA adapters
LPT1
COM1
COM2
Floppy
KBD
Keyboard
SoundBlaster sound board
Other 16 bit adapters
Ultra DMA harddisks, Zip- and other drives
CD-ROM drives and recorders
PCI
EIDE controller
PCI adapters
FireWire controller
Graphics adapter
Network card
Other 32 bit adapters
SCSI controller
Harddisks, other drives, scanners ao.
High performance drives ao.
AGP
AGP slot
Graphics adapter
USB
USB-units and -hubs
Keyboard
Scanner
Digital camera

2. ISA BUS

ISA = Industry Standard Architecture

- ISA Bus (IBM) it's a ***synchronous bus*** all the generated cycles follow a fix clock

- The ISA Bus is **less *flexibile*** concerning the transfer rate, but allows to realize ***simple and cheep devices***

- *A card connected on ISA bus* ***cannot be a master.***

Bus	Transmission time	Data width
ISA	375 ns	16 bit
PCI	30 ns	32 bit

ISA Bus

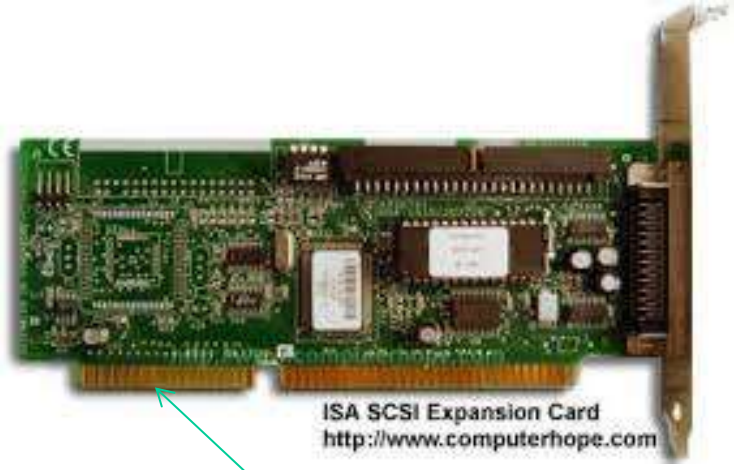
- Closely associated with the PC system bus

- **First ISA bus** (8-bit wide data path)
  Based on 8088 processor, It has 62 pins including:
    - 20 address lines
    - 8 data lines
    - 6 interrupt signals
    - Memory read, memory write
    - I/O read, and I/O write
    - 4 DMA requests and 4 DMA ACKs

- **16-bit ISA**

Added 36 pins to the 8-bit ISA bus (98)

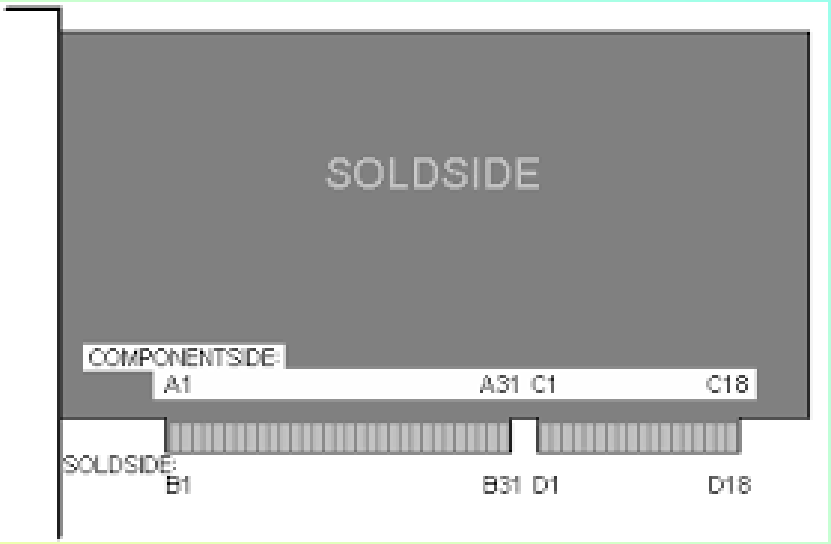
- 24 address lines
- 16 data lines
- Backward compatible with 8-bit ISA



ISA Bus (cont'd)

- Operates at 8.33 MHz
- Bandwidth of about 8 MB/s (8 bit ISA)
- 32-bit processors need more support
  - Several attempts were made to accommodate
    - EISA (Extended ISA)
      - Bus mastering signals
    - MCA (Micro Channel Architecture)
      - IBM proprietary
      - Never really took off
- ISA is used for older, slower I/O devices

3. ISA BUS SIGNALS



Signal	Pin	Pin	Signal
Ground	B1	A1	-I/O CH CHK
RESET DRV	B2	A2	Data Bit 7
+5 Vdc	B3	A3	Data Bit 6
IRQ 9	B4	A4	Data Bit 5
-5 Vdc	B5	A5	Data Bit 4
DRQ 2	B6	A6	Data Bit 3
-12 Vdc	B7	A7	Data Bit 2
-0 WAIT	B8	A8	Data Bit 1
+12 Vdc	B9	A9	Data Bit 0
Ground	B10	A10	-I/O CH RDY
-SMEMW	B11	A11	AEN
-SMEMR	B12	A12	Address 19
-IOW	B13	A13	Address 18
-IOR	B14	A14	Address 17
-DACK 3	B15	A15	Address 16
DRQ 3	B16	A16	Address 15
-DACK 1	B17	A17	Address 14
DRQ 1	B18	A18	Address 13
-Refresh	B19	A19	Address 12
CLK(8.33MHz)	B20	A20	Address 11
IRQ 7	B21	A21	Address 10
IRQ 6	B22	A22	Address 9
IRQ 5	B23	A23	Address 8
IRQ 4	B24	A24	Address 7
IRQ 3	B25	A25	Address 6
-DACK 2	B26	A26	Address 5
T/C	B27	A27	Address 4
BALE	B28	A28	Address 3
+5 Vdc	B29	A29	Address 2
OSC(14.3MHz)	B30	A30	Address 1
Ground	B31	A31	Address 0

-MEM CS16	D1	C1	-SBHE
-I/O CS16	D2	C2	Latch Address 23
IRQ 10	D3	C3	Latch Address 22
IRQ 11	D4	C4	Latch Address 21
IRQ 12	D5	C5	Latch Address 20
IRQ 15	D6	C6	Latch Address 19
IRQ 14	D7	C7	Latch Address 18
-DACK 0	D8	C8	Latch Address 17
DRQ 0	D9	C9	-MEMR
-DACK 5	D10	C10	-MEMW
DRQ5	D11	C11	Data Bit 8
-DACK 6	D12	C12	Data Bit 9
DRQ 6	D13	C13	Data Bit 10
-DACK 7	D14	C14	Data Bit 11
DRQ 7	D15	C15	Data Bit 12
+5 Vdc	D16	C16	Data Bit 13
-Master	D17	C17	Data Bit 14
Ground	D18	C18	Data Bit 15

SA19 to SA0

System Address bits 19:0 are used to address memory and I/O devices within the system. These signals may be used along with LA23 to LA17 to address up to 16MB of memory. Only the lower 16 bits are used during I/O operations to address up to 64K I/O locations. These signals are gated on the system bus when BALE is high and are latched on the falling edge of BALE. They remain valid throughout a read or write command. These signals are normally driven by the system microprocessor or DMA controller.

LA23 to LA17

Unlatched Address bits 23:17 are used to address memory within the system. They are used along with SA19 to SA0 to address up to 16 MB of memory. These signals are valid when BALE is high. They are "unlatched" and do not stay valid for the entire bus cycle. Decodes of these signals should be latched on the falling edge of BALE.

AEN

Address Enable is used to disable the system microprocessor and other devices from the bus during DMA transfers. When this signal is active the system DMAC has control of the address, data, and read/write signals. This signal should be included as part of ISA board select decodes to prevent incorrect board selects during DMA cycles.

BALE
Buffered Address Latch Enable is used to latch the LA23 to LA17 signals or decodes of these signals. Addresses are latched on the falling edge of BALE. It is forced high during DMA cycles. When used with AEN, it indicates a valid microprocessor or DMA address.

CLK
System Clock is a freerunning clock typically in the 8.33MHz range, although its exact frequency is not guaranteed. It is used in some ISA board applications to allow synchronization with the system microprocessor.

-SMEMR
System Memory Read - select a memory device to drive data onto the data bus. It is active only when the memory decode is within the low 1 MB of memory space. SMEMR is derived from MEMR and a decode of the low 1 MB of memory.

-SMEMW
System Memory Write -select a memory device to store the data currently on the data bus. It is active only when the memory decode is within the low 1 MB of memory space. SMEMW is derived from MEMW and a decode of the low 1 MB of memory.

-MEMR
Memory Read select a memory device to drive data onto the data bus. It is active on all memory read cycles.

-MEMW
Memory Write select a memory device to store the data currently on the data bus. It is active on all memory write cycles.

-REFRESH *Memory Refresh* is driven low to indicate a memory refresh operation is in progress.

OSC *Oscillator* is a clock with a 70ns period (14.31818 MHz). This signal is not synchronous with the system clock (CLK).

RESET DRV *Reset Drive* is driven high to reset or initialize system logic upon power up or subsequent system reset.

SD15 to SD0
System Data serves as the data bus bits for devices on the ISA bus. SD7 - SD0 are used for transfer of data with 8-bit devices. SD15 - SD0 are used for transfer of data with 16-bit devices. 16-bit devices transferring data with 8-bit devices shall convert the transfer into two 8-bit cycles using SD7 - SD0.

-DACK0 to -DACK3 and -DACK5 to -DACK7
DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests on DRQ0 to DRQ3 and DRQ5 to DRQ7.

DRQ0 to DRQ3 and DRQ5 to DRQ7
DMA Requests are used by ISA boards to request service from the system DMA controller or to request ownership of the bus as a bus master device. These signals may be asserted asynchronously. The requesting device must hold the request signal active until the system board asserts the corresponding DACK signal.

-I/O CH CK *I/O Channel Check* signal may be activated by ISA boards to request than an non-maskable interrupt (NMI) be generated to the system microprocessor. It is driven active to indicate a uncorrectable error has been detected.

I/O CH RDY *I/O Channel Ready* allows slower ISA boards to lengthen I/O or memory cycles by inserting wait states. This signals normal state is active high (ready). ISA boards drive the signal inactive low (not ready) to insert wait states. Devices using this signal to insert wait states should drive it low immediately after detecting a valid address decode and an active read or write command. The signal is release high when the device is ready to complete the cycle.

-IOR *I/O Read* is driven by the owner of the bus and instructs the selected I/O device to drive read data onto the data bus.

-IOW *I/O Write* is driven by the owner of the bus and instructs the selected I/O device to capture the write data on the data bus.

IRQ3 to IRQ7 and IRQ9 to IRQ12 and IRQ14 to IRQ15 *Interrupt Requests* are used to signal the system microprocessor that an ISA board requires attention. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the request through its interrupt service routine. These signals are prioritized with IRQ9 to IRQ12 and IRQ14 to IRQ15 having the highest priority (IRQ9 is the highest) and IRQ3 to IRQ 7 have the lowest priority (IRQ7 is the lowest).

TC *Terminal Count* provides a pulse to signal a terminal count has been reached on a DMA channel operation.

-MASTER

Master is used by an ISA board along with a DRQ line to gain ownership of the ISA bus. Upon receiving a -DACK a device can pull -MASTER low which will allow it to control the system address, data, and control lines. After -MASTER is low, the device should wait one CLK period before driving the address and data lines, and two clock periods before issuing a read or write command.

-MEM CS16

Memory Chip Select 16 is driven low by a memory slave device to indicate it is capable of performing a 16-bit memory data transfer.

-I/O CS16

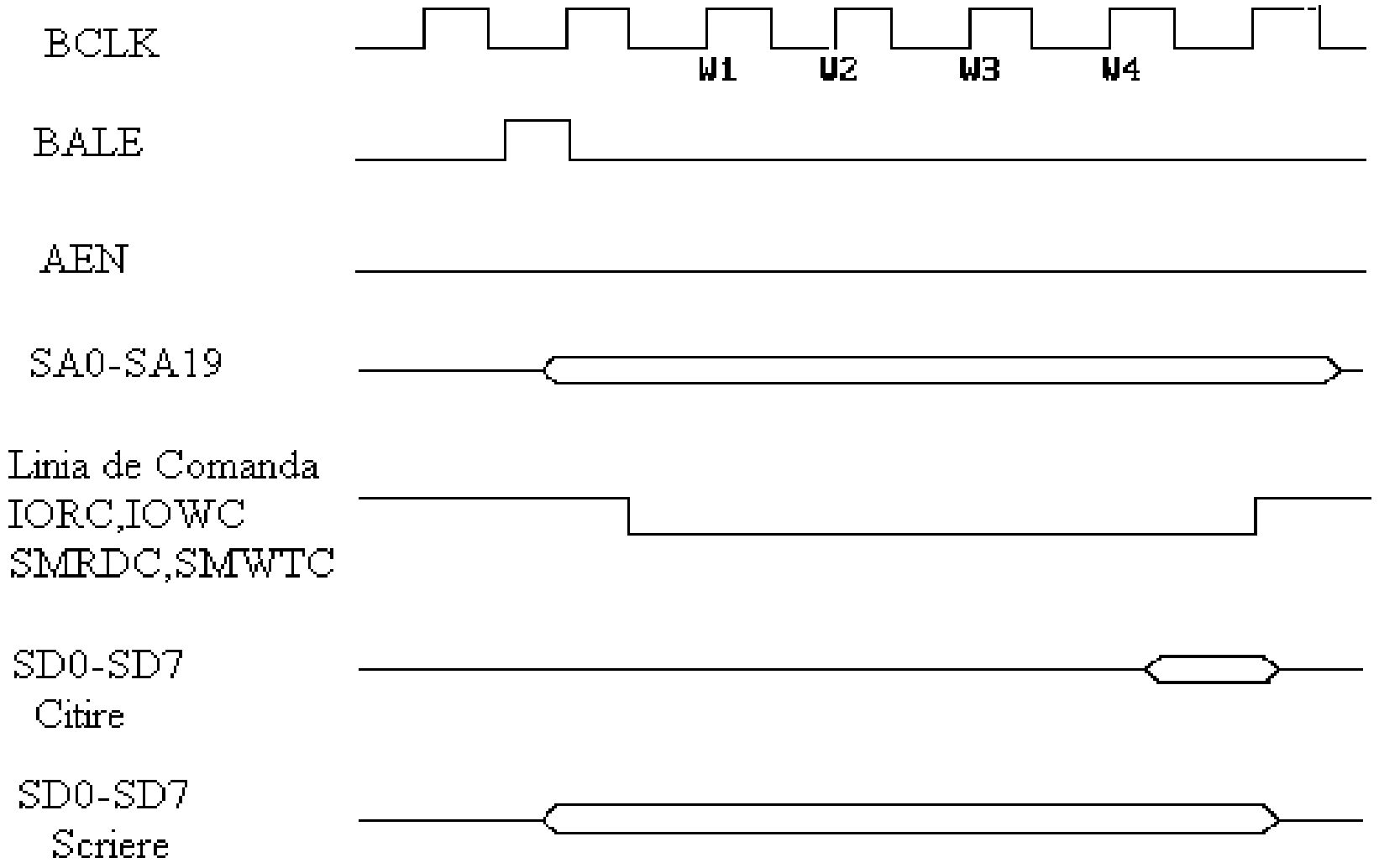
I/O Chip Select 16 is driven low by a I/O slave device to indicate it is capable of performing a 16-bit I/O data transfer. This signal is driven from a decode of the SA15 to SA0 address lines.

-0WS

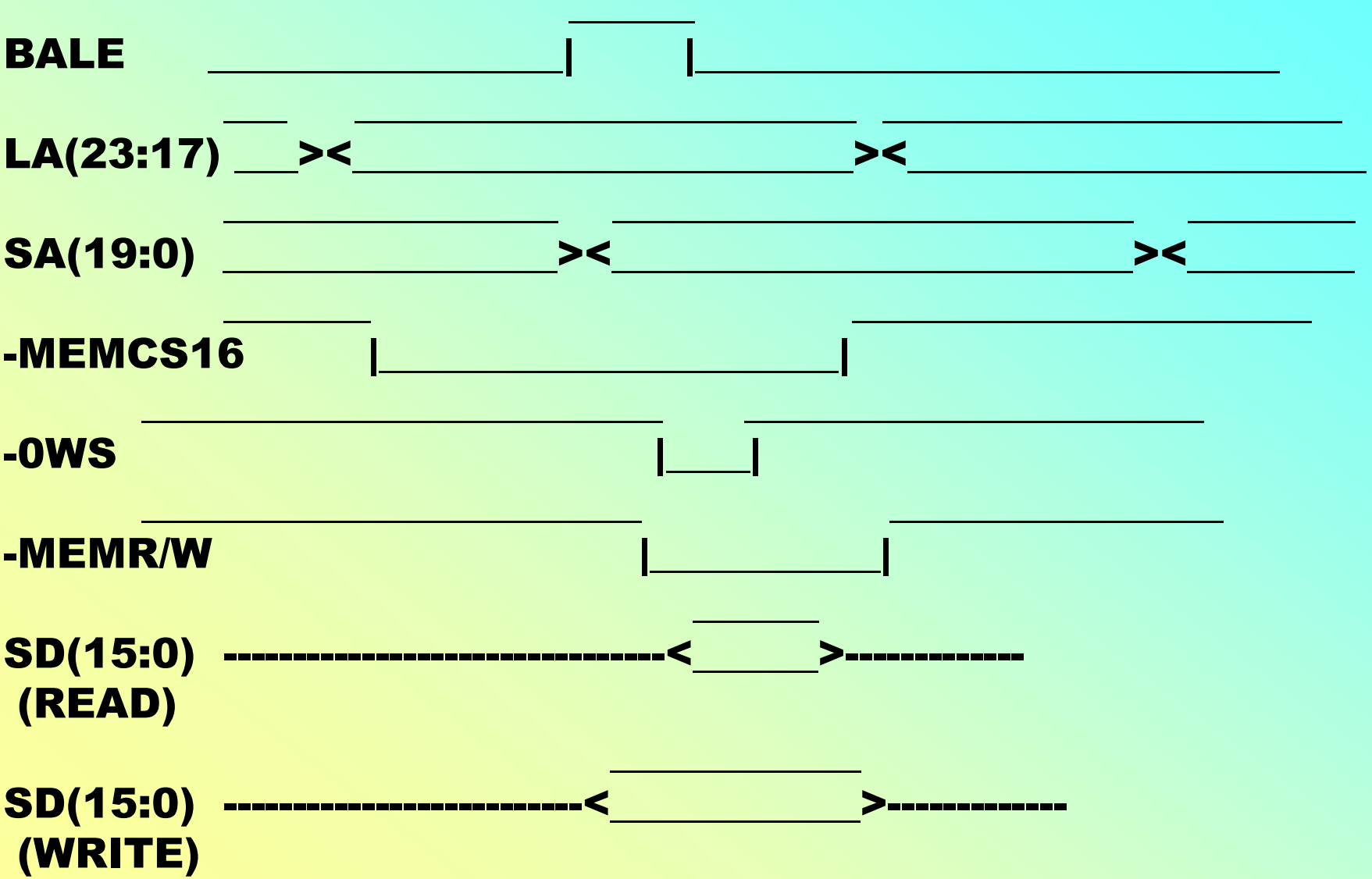
Zero Wait State is driven low by a bus slave device to indicate it is capable of performing a bus cycle without inserting any additional wait states. To perform a 16-bit memory cycle without wait states, -0WS is derived from an address decoder.

-SBHE

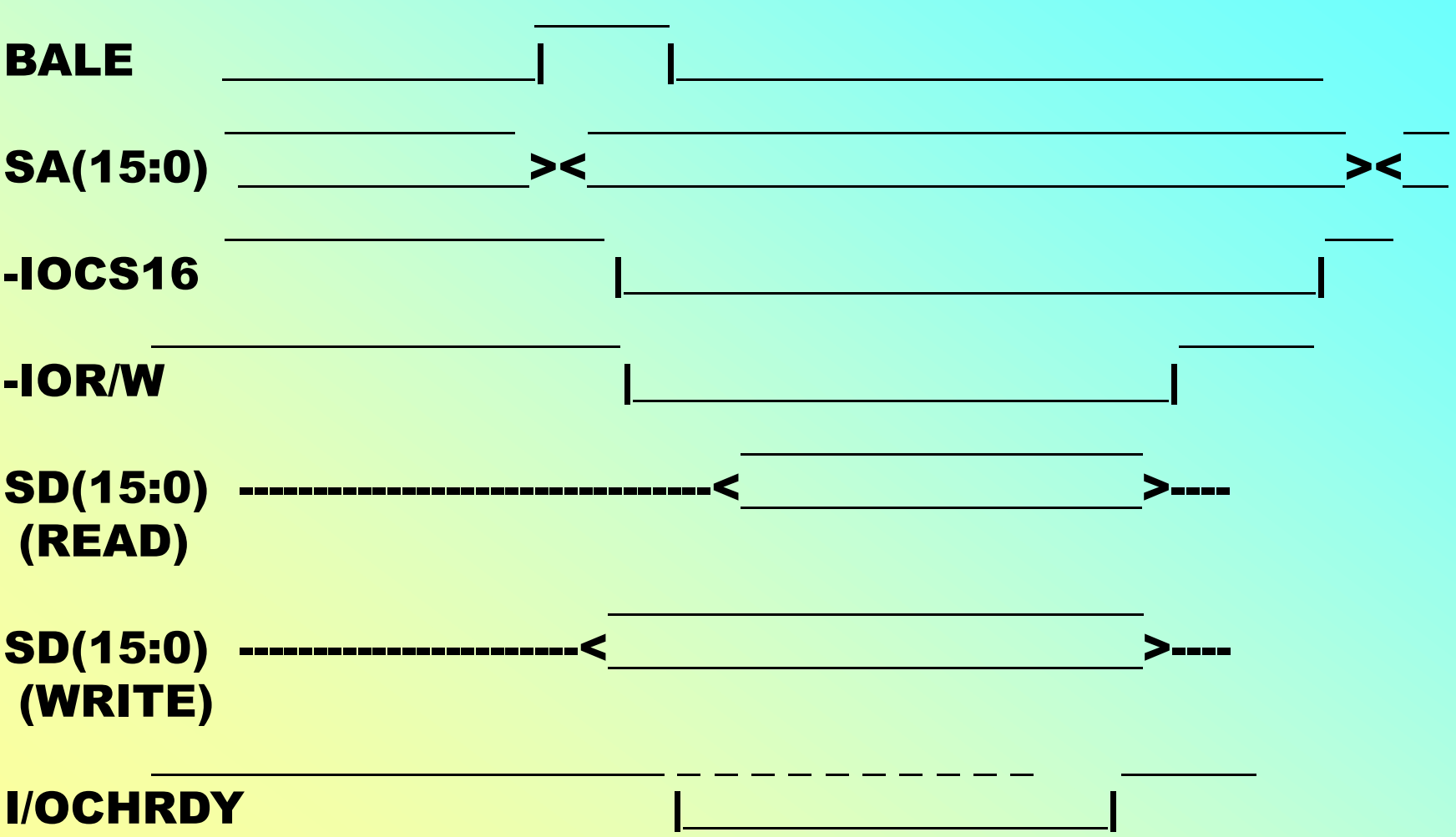
System Byte High Enable is driven low to indicate a transfer of data on the high half of the data bus (D15 to D8).


BCLK
W1
W2
W3
W4
BALE
AEN
SA0-SA19
Linia de Comanda
IORC,IOWC
SMRDC,SMWTC
SD0-SD7
Citire
SD0-SD7
Scriere

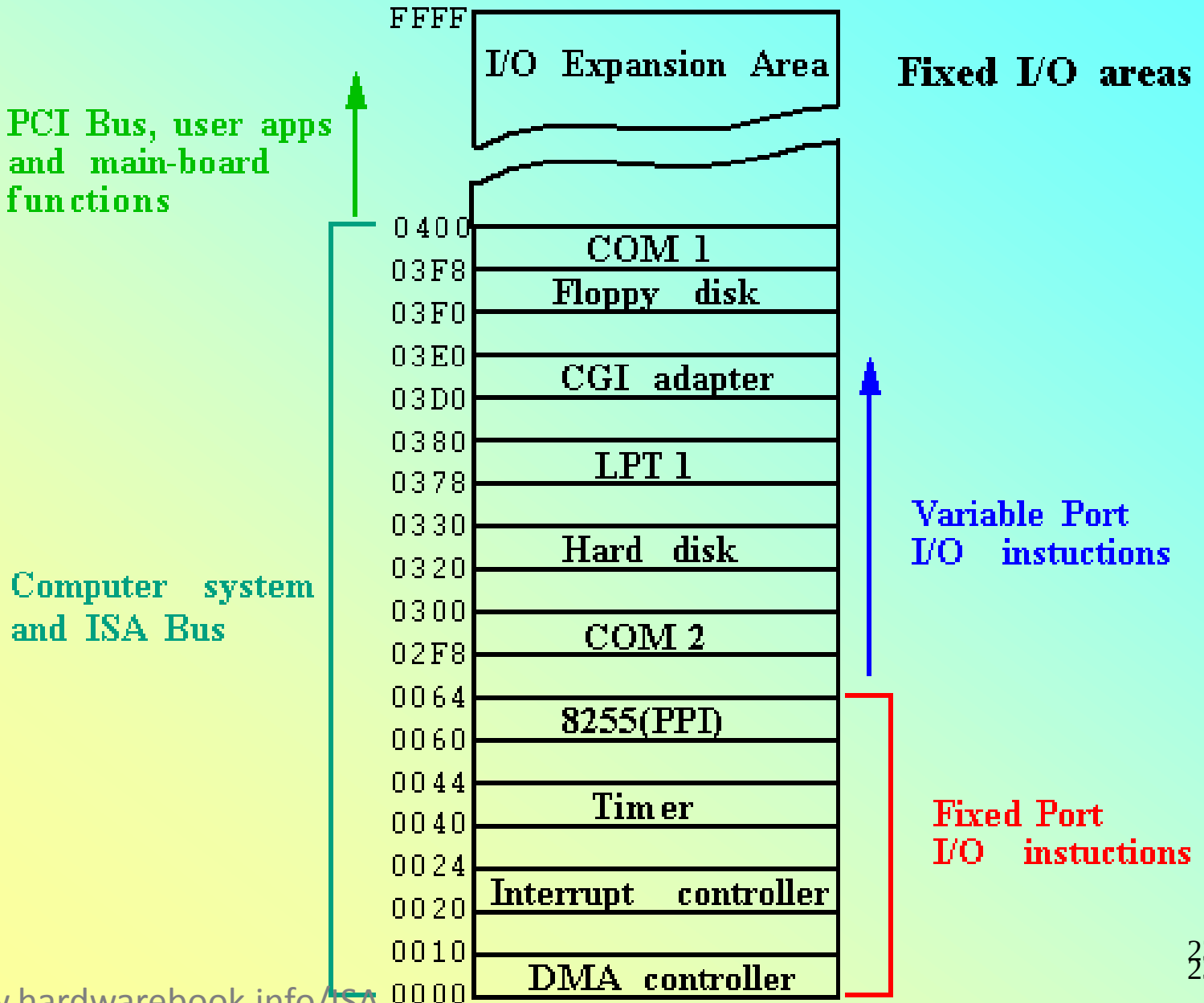
16-Bit Memory Bus Cycles (0 Wait State)



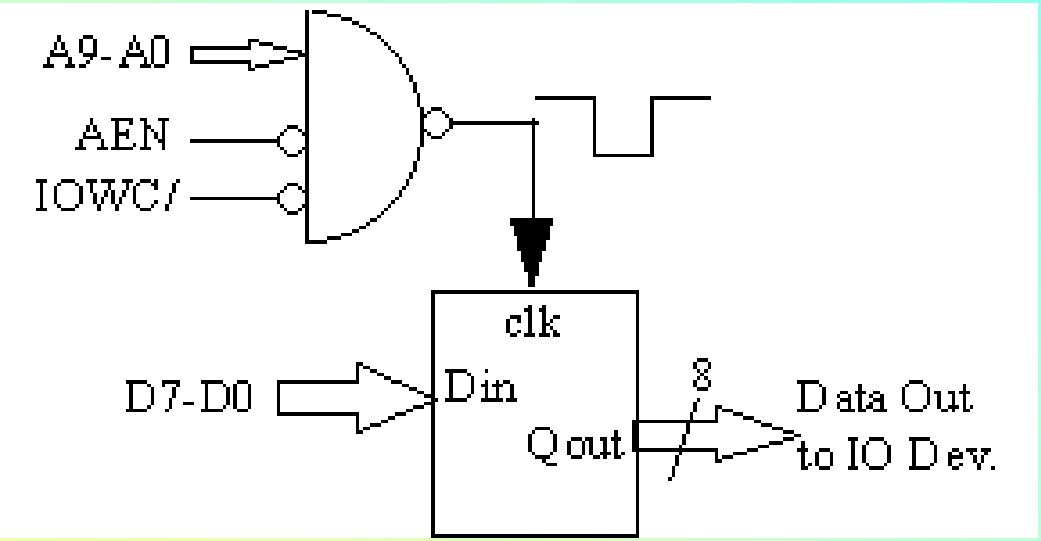
16-Bit I/O Bus Cycles



4. ISA Interface Design

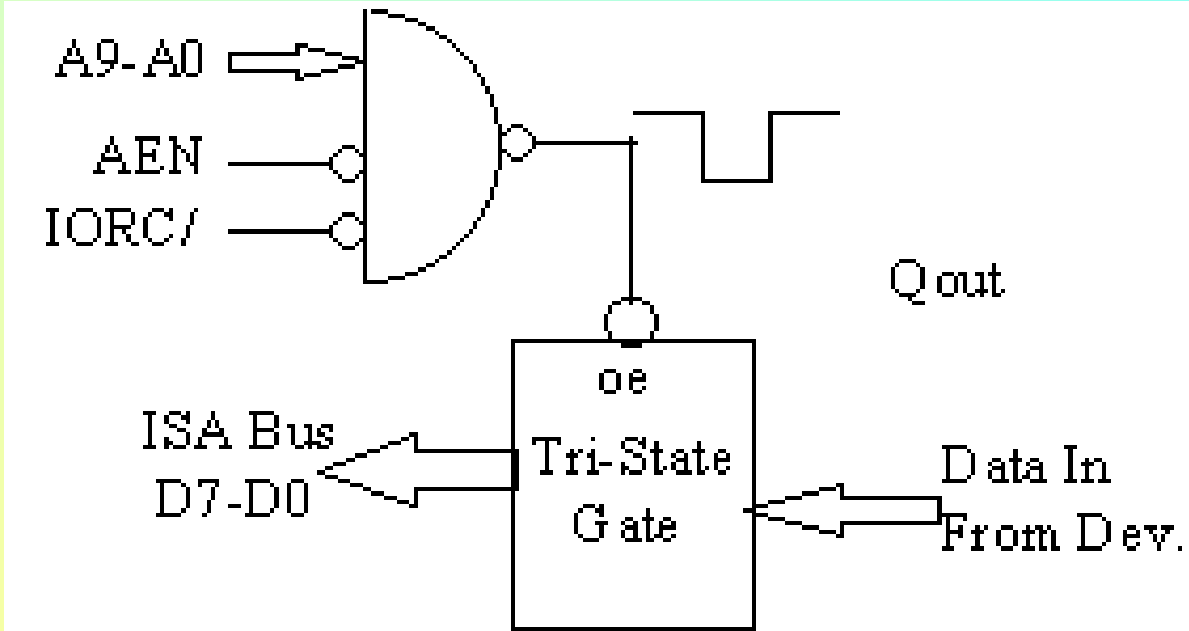


23



Simple Output Port Design

Simple Input Port Design



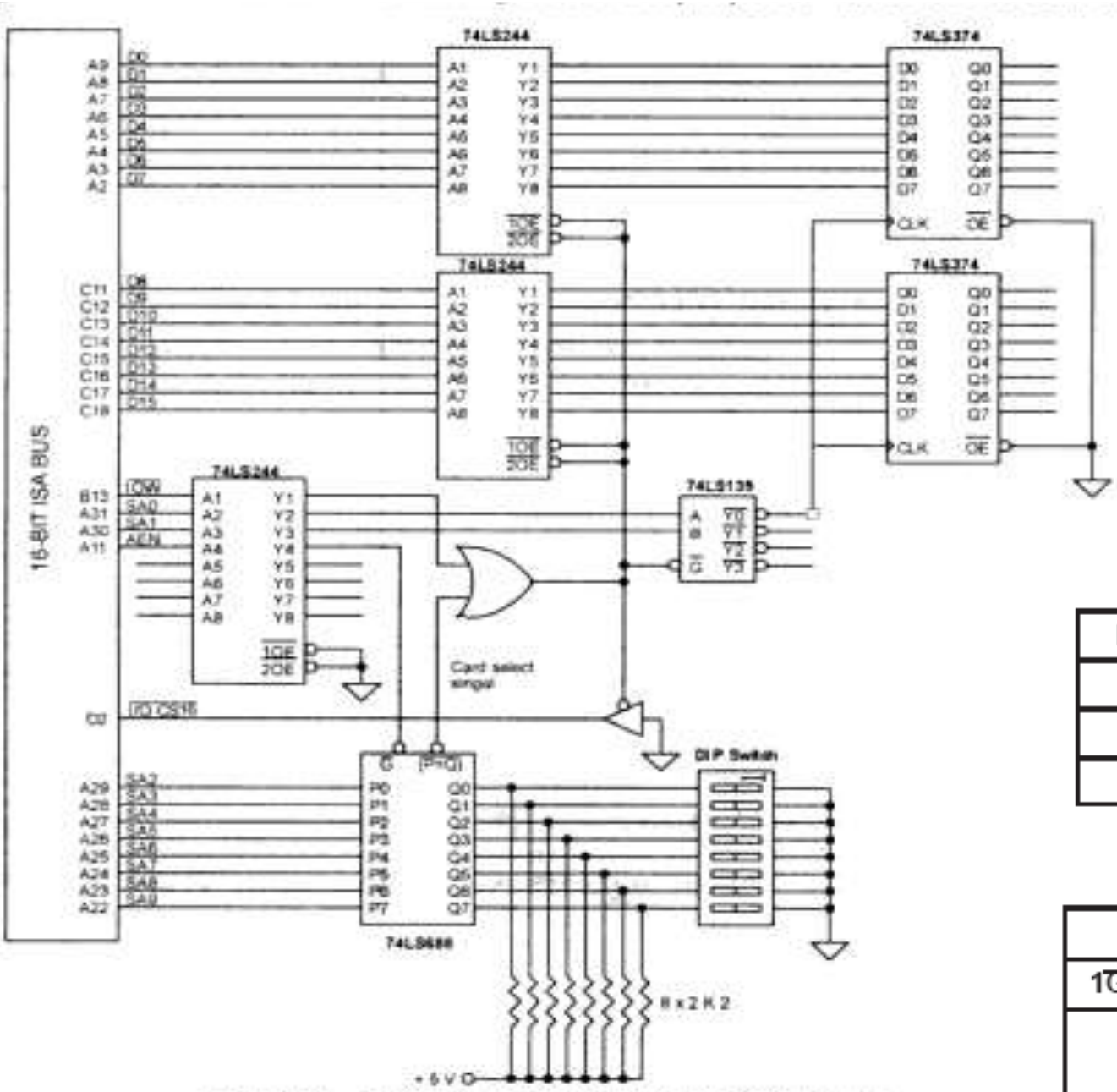


Figure 9.9 Interfacing 16-bit output port to 16-bit ISA bus.

LS374

D_n	LE	$\overline{OE}$	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z*

SN74LS244

INPUTS		OUTPUT
$1\overline{G}$, $2\overline{G}$	D	
L	L	L
L	H	H
H	X	(Z)

Limits of the ISA BUS

- Speed (8.33MHz)
- Data width (8/16b)
- Access time to the I/O devices
- Performances (~5MB/s-~10MB/s)

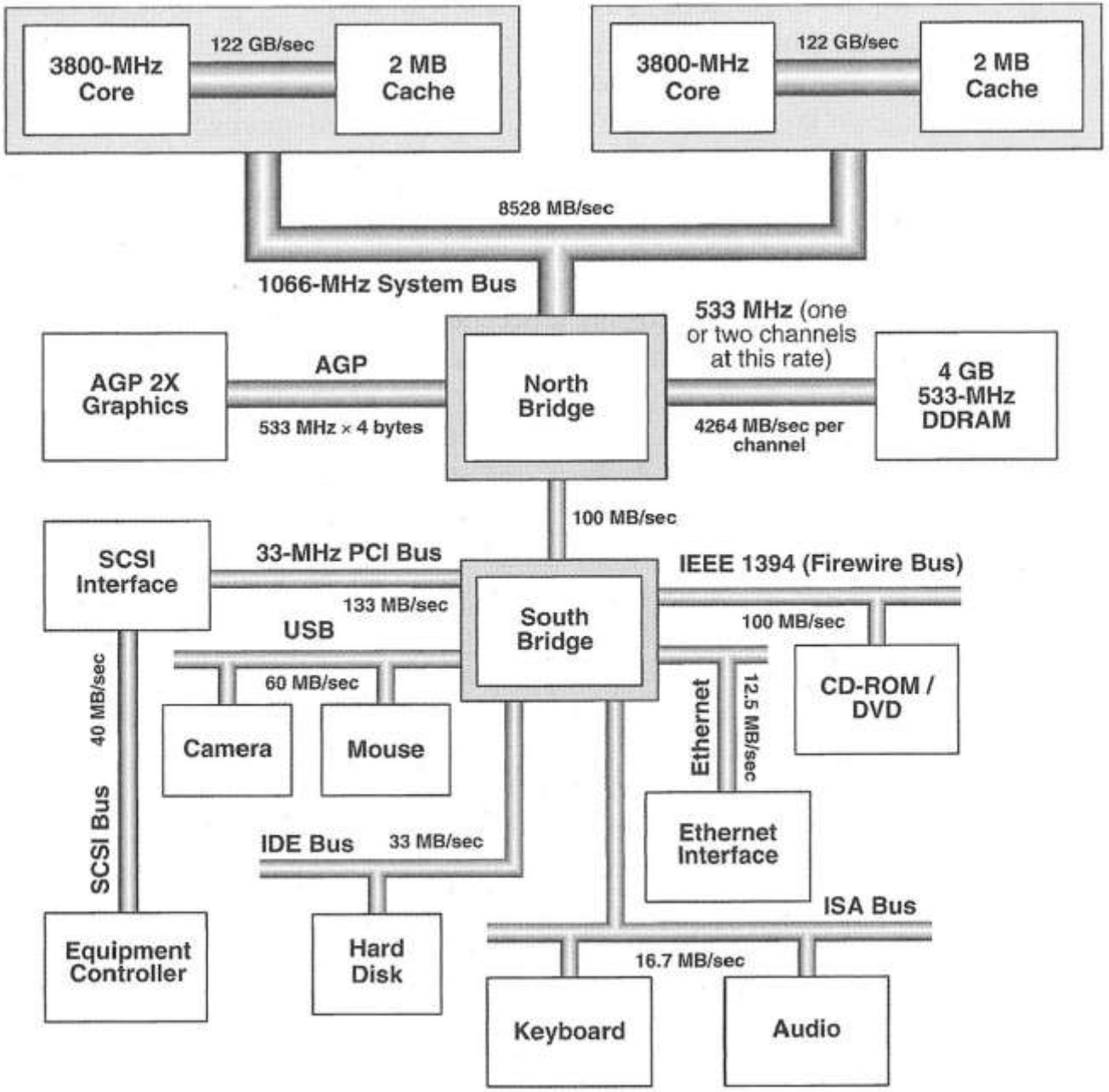


Figure 8-7
Bridging with dual Pentium processors. (Source: http://www.intel.com.)