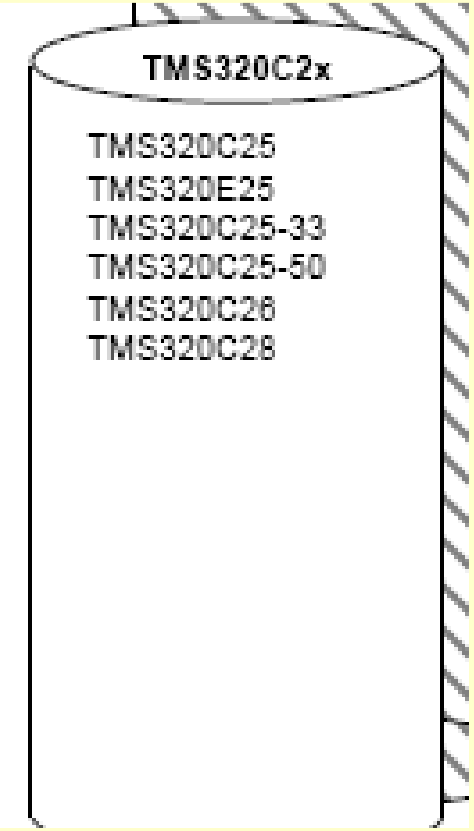
C4. TMS320C25



Outline :

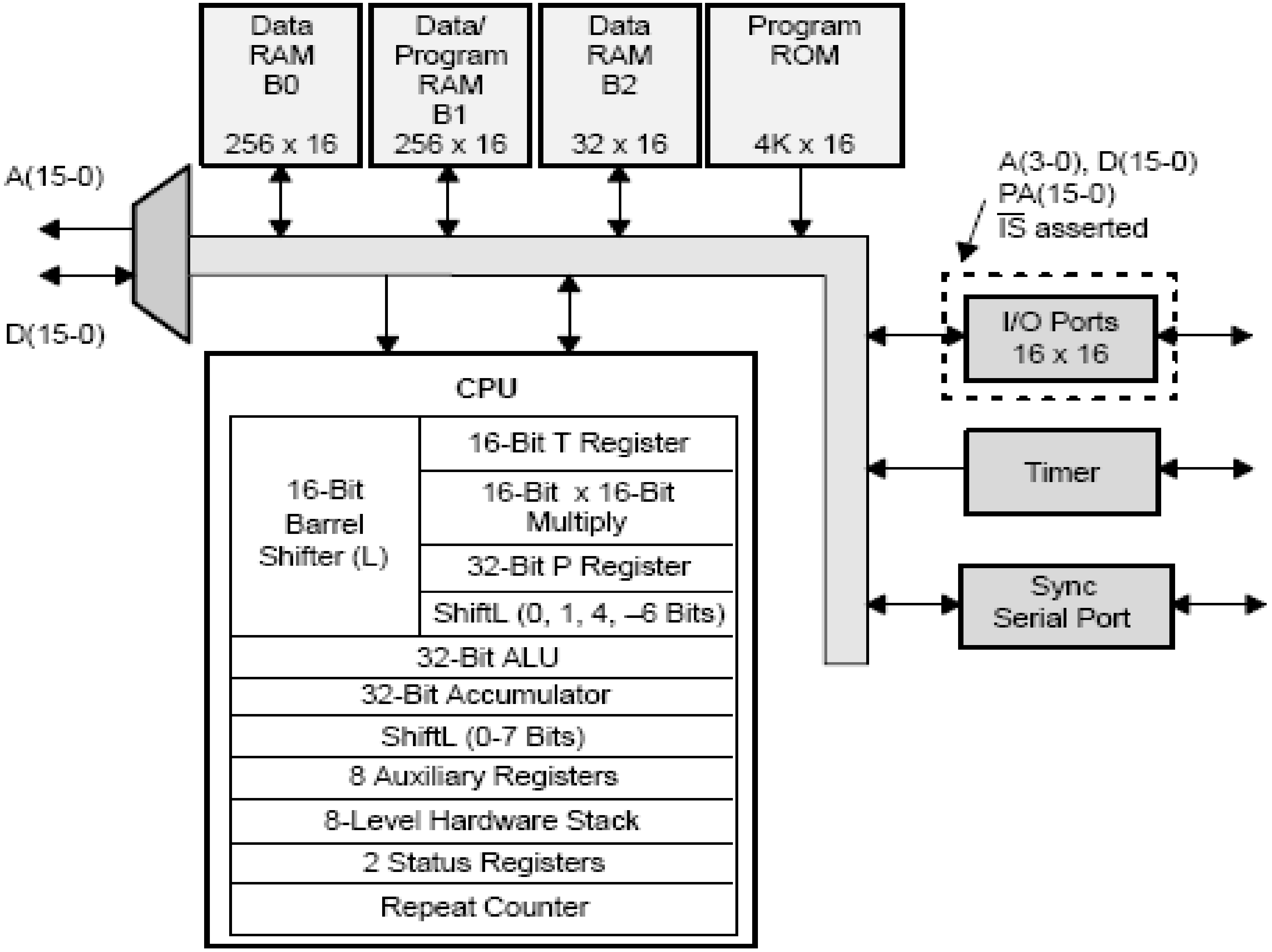
- TMS320C2x family
- TMS320C25 Block Diagram - Details
- TMS320C2x Signal Descriptions

Reference: SPRU014C.pdf

Main Features

- Harvard architecture
- ALU
- Multiplier 16x16/1 cycle
- Memory interface
- Serial ports
- Multiprocessing applications
- Direct Memory Access

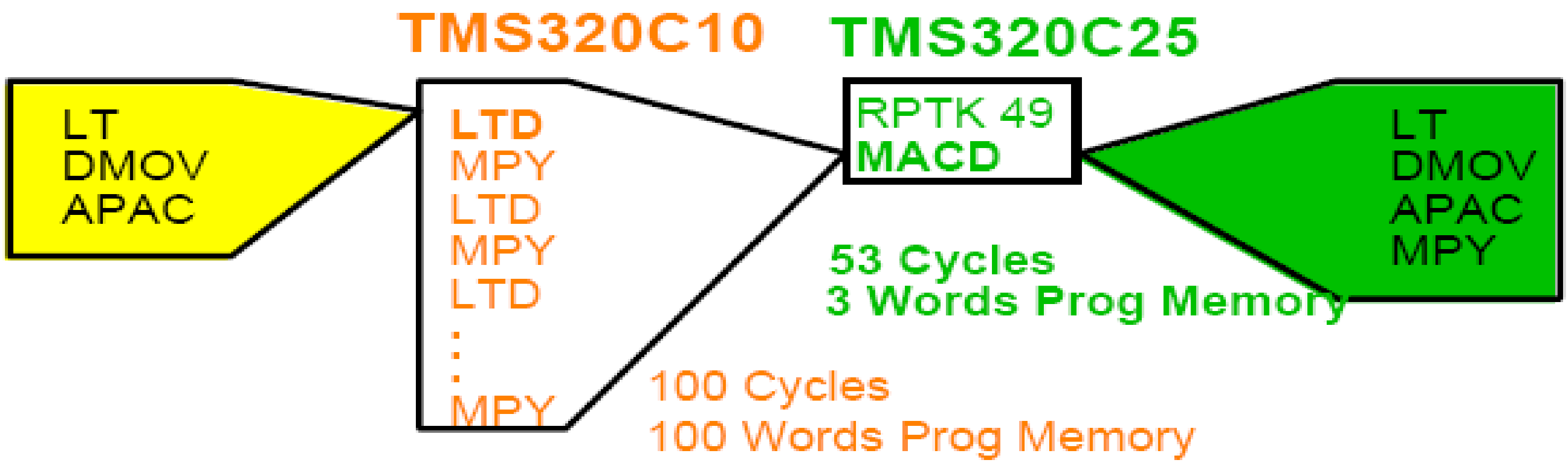
TMS320C25 Block Diagram



TMS320C2x Processors Overview

Device	Memory: On-chip RAM	Memory: ROM/EPROM	Memory: Off-chip Prog	Memory: Off-chip Data	I/O Ports †: Ser	I/O Ports †: Par	I/O Ports †: DMA	Cycle Time (ns)	Package Type*: PGA	Package Type*: PLCC	Package Type*: CER	Package Type*: QFP
TMS320C25‡	544	4K	64K	64K	Yes	16 × 16	Con	100	68	68	—	—
TMS320C25-33	544	4K	64K	64K	Yes	16 × 16	Con	120	—	68	—	—
TMS320C25-50§	544	4K	64K	64K	Yes	16 × 16	Con	80	—	68	—	—
TMS320E25§	544	4K	64K	64K	Yes	16 × 16	Con	100	—	—	68	80
TMS320C26	1568	256	64K	64K	Yes	16 × 16	Con	100	—	68	—	—
TMS320C28	544	8K	64K	64K	Yes	16 × 16	Con	100	—	68	—	80

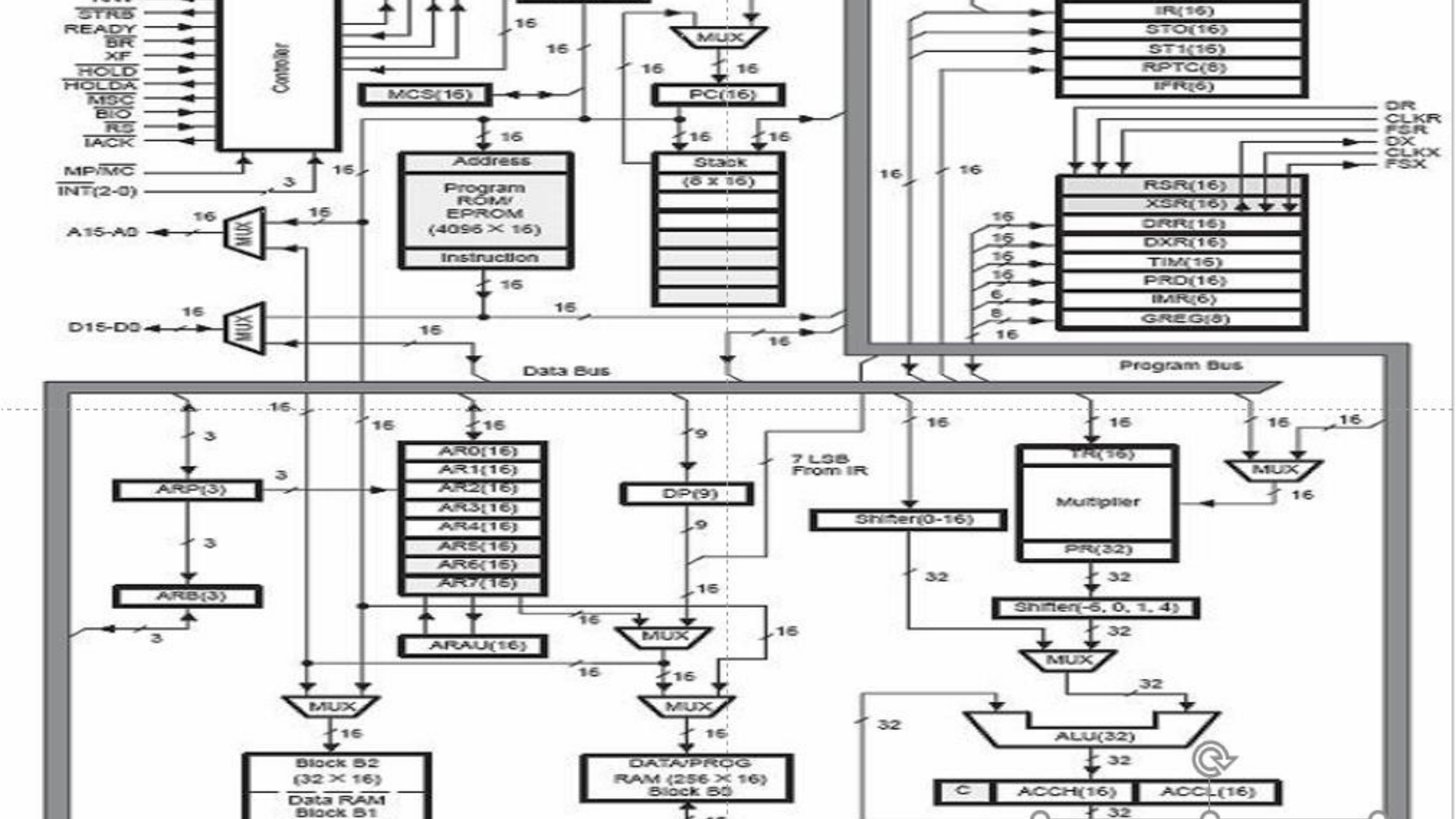
Single Cycle Multiply - Accumulate!



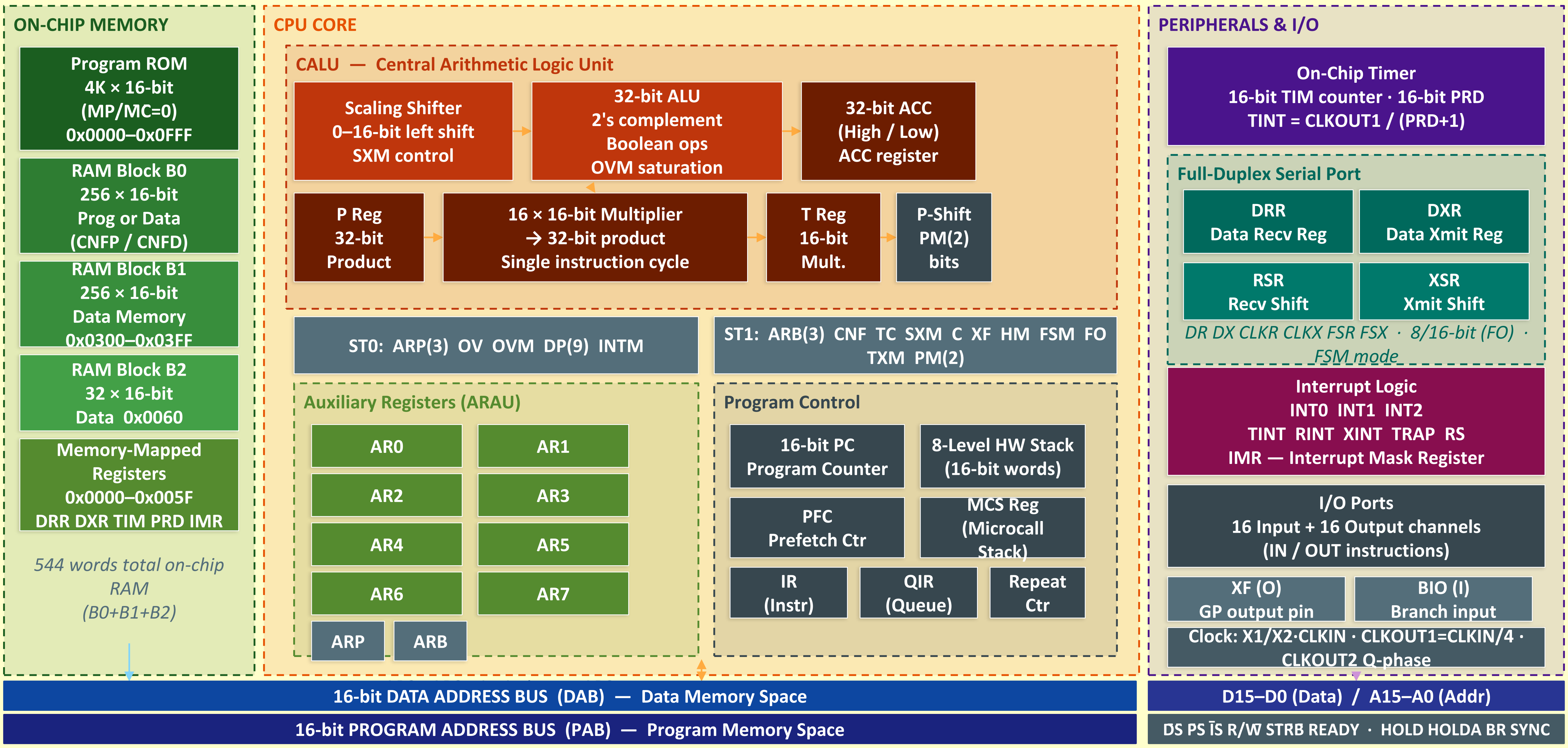
Key Features of TMS320C2x family

- Harvard Architecture
- Instruction cycle timing: ~25ns (TMS320C25)
- 544-word programmable on-chip data RAM
- 4Kword on-chip program ROM
- 128Kword data/program memory space
- 32-bit ALU/accumulator
- 16 × 16-bit parallel multiplier with a 32-bit product
- Single-cycle multiply/accumulate instructions
- Repeat instructions for efficient use of program space and enhanced execution
- Block moves for data/program management
- On-chip timer for control operations
- 8 auxiliary registers (AR) with a dedicated arithmetic unit (ARAU)
- 8-level hardware stack
- 16 input+16 output channels (I/O)
- 16-bit parallel shifter
- Wait states for communication to slower off-chip memories/peripherals
- Serial port for direct codec (AIC) interface
- Synchronization input for synchronous multiprocessor configurations
- Global data memory interface
- TMS320C1x source-code upward compatibility
- Instructions for adaptive filtering, FFT, and extended-precision arithmetic
- Bit-reversed indexed-addressing mode for radix-2 FFT
- On-chip clock generator, Single 5V supply, 68-pin PGA/PLCC (TMS320C25) package

- **Harvard Architecture-**The TMS320C2x implement a Harvard-type architecture that maximizes processing power by maintaining two separate memory bus structures, program and data;
- **On-Chip Memory -** The TMS320C25 provides increased flexibility in system design by two large on-chip data *RAM blocks* (a total of *544x 16-bit words),* one of which is configurable either as program or data memory, the large on-chip *4K-word masked ROM* on the TMS320C25 can reduce the cost of systems, thus providing for a true single-chip DSP solution
- **Arithmetic Logic Unit -** The TMS320C2x performs 2's complement arithmetic using the 32-bit ALU and accumulator. The ALU is a general-purpose arithmetic unit that operates using 16-bit words taken from data RAM or derived from immediate instructions or using the 32-bit result of the multiplier's product register. Also, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.
- **Multiplier.** The multiplier performs a 16×16 bit, 2s-complement multiplication with a 32-bit result in a single instruction cycle. The multiplier consists of three elements***: the T register, P register, and multiplier array (hardware)*.**
- **Memory, I/O Interface.** The TMS320C2x local memory interface consists of a 16-bit ***parallel data bus*** (D15–D0), a 16-bit ***address bus*** (A15–A0), three pins for data/program memory or I/O space select (DS, PS, and IS), and various system control signals.
- **Serial Port.** An on-chip *full-duplex serial port* (8/16 bits) provides direct communication with serial devices such as codecs, serial A/D converters and other serial systems.
- **Multiprocessing Applications.** The TMS320C2x has the capability of allocating *global data memory* space and communicating with that space via the (bus request) and READY signals.
- **Direct Memory Access.** The TMS320C2x supports direct memory access (DMA) to its external program/data memory using the HOLD and HOLDA signals.



STRB
READY
BR
XF
HOLD
HOLDA
MSC
BIO
RS
IACK
MP/MC
INT(2-0)
A15-A0
D15-D0
Controller
MCS(16)
MUX
PC(16)
Address
Program ROM/ EPROM (4096 × 16)
Instruction
Stack (8 x 16)
IR(16)
ST0(16)
ST1(16)
RPTC(8)
IFR(6)
DR
CLKR
FSR
DX
CLKX
FSX
RSR(16)
XSR(16)
DRR(16)
DXR(16)
TIM(16)
PRD(16)
IMR(6)
GREG(8)
Data Bus
Program Bus
ARP(3)
ARB(3)
AR0(16)
AR1(16)
AR2(16)
AR3(16)
AR4(16)
AR5(16)
AR6(16)
AR7(16)
ARAU(16)
DP(9)
7 LSB From IR
Shifter(0-16)
TR(16)
Multiplier
PR(32)
Shifter(-6, 0, 1, 4)
ALU(32)
C
ACCH(16)
ACCL(16)
Block B2 (32 × 16)
Data RAM Block B1
DATA/PROG RAM (256 × 16) Block B0


ON-CHIP MEMORY
Program ROM
4K × 16-bit
(MP/MC=0)
0x0000–0x0FFF
RAM Block B0
256 × 16-bit
Prog or Data
(CNFP / CNFD)
RAM Block B1
256 × 16-bit
Data Memory
0x0300–0x03FF
RAM Block B2
32 × 16-bit
Data 0x0060
Memory-Mapped
Registers
0x0000–0x005F
DRR DXR TIM PRD IMR
544 words total on-chip RAM (B0+B1+B2)
CPU CORE
CALU — Central Arithmetic Logic Unit
Scaling Shifter
0–16-bit left shift
SXM control
32-bit ALU
2's complement
Boolean ops
OVM saturation
32-bit ACC
(High / Low)
ACC register
P Reg
32-bit
Product
16 × 16-bit Multiplier
→ 32-bit product
Single instruction cycle
T Reg
16-bit
Mult.
P-Shift
PM(2)
bits
ST0: ARP(3) OV OVM DP(9) INTM
ST1: ARB(3) CNF TC SXM C XF HM FSM FO TXM PM(2)
Auxiliary Registers (ARAU)
AR0
AR1
AR2
AR3
AR4
AR5
AR6
AR7
ARP
ARB
Program Control
16-bit PC
Program Counter
8-Level HW Stack
(16-bit words)
PFC
Prefetch Ctr
MCS Reg
(Microcall Stack)
IR
(Instr)
QIR
(Queue)
Repeat
Ctr
PERIPHERALS & I/O
On-Chip Timer
16-bit TIM counter · 16-bit PRD
TINT = CLKOUT1 / (PRD+1)
Full-Duplex Serial Port
DRR
Data Recv Reg
DXR
Data Xmit Reg
RSR
Recv Shift
XSR
Xmit Shift
DR DX CLKR CLKX FSR FSX · 8/16-bit (FO) · FSM mode
Interrupt Logic
INT0 INT1 INT2
TINT RINT XINT TRAP RS
IMR — Interrupt Mask Register
I/O Ports
16 Input + 16 Output channels
(IN / OUT instructions)
XF (O)
GP output pin
BIO (I)
Branch input
Clock: X1/X2·CLKIN · CLKOUT1=CLKIN/4 · CLKOUT2 Q-phase
16-bit DATA ADDRESS BUS (DAB) — Data Memory Space
16-bit PROGRAM ADDRESS BUS (PAB) — Program Memory Space
D15–D0 (Data) / A15–A0 (Addr)
DS PS IS R/W STRB READY · HOLD HOLDA BR SYNC

TMS320C2x Internal Hardware*

Unit	Symbol	Function
Accumulator	ACC (31–0) ACCH (31–16) ACCL (15–0)	A 32-bit accumulator split in two halves: ACCH (accumulator high) and ACCL (accumulator low). Used for storage of ALU output.
Arithmetic Logic Unit	ALU	A 32-bit twos-complement arithmetic logic unit having two 32-bit input ports and one 32-bit output port feeding the accumulator.
Auxiliary Register Arithmetic Unit	ARAU	A 16-bit unsigned arithmetic unit used to perform operations on auxiliary register data.
Auxiliary Register File	AR0–AR7 (15–0)	A register file containing eight 16-bit auxiliary registers (AR0–AR7), used for addressing data memory, temporary storage, or integer arithmetic processing through the ARAU.
Auxiliary Register File Bus	AFB(15–0)	A 16-bit bus that carries data from the AR pointed to by the ARP.
Auxiliary Register Pointer	ARP(2–0)	A 3-bit register used to select one of five or eight auxiliary registers.
Auxiliary Register Pointer Buffer	ARB(2–0)	A 3-bit register used to buffer the ARP. Each time the ARP is loaded, the old value is written to the ARB, except during an LST (load status register) instruction. When the ARB is loaded with an LST1, the same value is also copied into ARP.
Central Arithmetic Logic Unit	CALU	The grouping of the ALU, multiplier, accumulator, and scaling shifter.
Data Bus	D(15–0)	A 16-bit bus used to route data.
Data Memory Address Bus	DAB(15–0)	A 16-bit bus that carries the data memory address.

Direct Data Memory Address Bus	DRB(15–0)	A 16-bit bus that carries the direct address for the data memory, which is the concatenation of the DP register with the seven LSBs of the instruction.
Global Memory Allocation Register	GREG(7–0)	An 8-bit memory-mapped register for allocating the size of the global memory space.

Unit	Symbol	Function
Instruction Register	IR(15–0)	A 16-bit register used to store the currently executing instruction.
Interrupt Flag Register	IFR(5–0)	A 6-bit flag register used to latch the active-low external user interrupts $\overline{\text{INT}}$(2–0), the internal interrupts XINT/RINT (serial port transmit/receive), and TINT (timer) interrupts. The IFR is not accessible through software.
Interrupt Mask Register	IMR(5–0)	A 6-bit memory-mapped register used to mask interrupts.
Microcall Stack	MCS (15–0)	A single-word stack that temporarily stores the contents of the PFC while the PFC is being used to address data memory with the block move (BLKD/BLKP), multiply-accumulate (MAC/MACD), and table read/write (TBLR/TBLW)and table read/write (TBLR/TBLW) instruction
Multiplier	MULT	A 16 × 16-bit parallel multiplier.
Period Register	PRD (15–0)	A 16-bit memory-mapped register used to reload the timer.
Prefetch Counter	PFC (15–0)	A 16-bit counter used to prefetch program instructions. The PFC contains the address of the instruction currently being prefetched. It is updated when a new prefetch is initiated. The PFC is also used to address program memory when using the block move (BLKP), multiply-accumulate (MAC/MACD), and table read/write (TBLR/TBLW) instructions and to address data memory when using the block move (BLKD) instruction.

TMS320C2x Internal Hardware

TMS320C2x Internal Hardware

Program Bus	P(15–0)	A 16-bit bus used to route instructions (and data for the MAC and MACD instructions).
Program Counter	PC (15–0)	A 16-bit program counter used to address program memory. The PC always contains the address of the next instruction to be executed. The PC contents are updated following each instruction decode operation.
Program Memory Address Bus	PAB(15–0)	A 16-bit bus that carries the program memory address.
Queue Instruction Register	QIR(15–0)	A 16-bit register used to store prefetched instructions.
Random Access Memory (data or program)	RAM (B0)	A RAM block with 256 × 16 locations configured as either data or program memory. (512 × 16 for TMS320C26)
Random Access Memory (data only)	RAM (B1)	A data RAM block, organized as 256 × 16 locations. (512 × 16 can be configured as program or data for TMS320C26)
Random Access Memory (data only)	RAM (B2)	A data RAM block, organized as 32 × 16 locations.
Random Access Memory (data or program)	RAM (B3) (TMS320C26 only)	A RAM block with 512 × 16 locations configured as either data or program memory (TMS320C26 only).
Read Only Memory	ROM	A ROM block, 4096 × 16 (256 × 16 for TMS320C26; 8192 × 16 for TMS320C28).
Repeat Counter	RPTC (7–0)	An 8-bit counter to control the repeated execution of a single instruction.

TMS320C2x Internal Hardware

Serial Port Data Receive Register	DRR(15–0)	A 16-bit memory-mapped serial port data receive register. Only the eight LSBs are used in the byte mode.
Serial Port Data Transmit Register	DXR(15–0)	A 16-bit memory-mapped serial port data transmit register. Only the eight LSBs are used in the byte mode.
Serial Port Receive Shift Register	RSR(15–0)	A 16-bit register used to shift in serial port data from the RX pin. RSR contents are sent to the DRR after a serial transfer is completed. RSR is not directly accessible through software.
Serial Port Transmit Shift Register	XSR(15–0)	A 16-bit register used to shift out serial port data onto the DX pin. XSR contents are loaded from DXR at the beginning of a serial port transmit operation. XSR is not directly accessible through software.
Shifters	—	Shifters are located at the ALU input, the accumulator output, and the product register output. Also, an in-place shifter is located within the accumulator.
Stack	Stack(15–0)	A 4 × 16 or 8 × 16 hardware stack used to store the PC during interrupts or calls. The ACCL and data memory values may also be pushed onto and popped from the stack.
Status Registers Temporary Register	ST0,ST1 (15–0)	Two 16-bit status registers that contain status and control bits. A 16-bit register that holds either an operand for the multiplier or a shift code for the scaling shifter.
Temporary Register	TR(15–0)	A 16-bit register that holds either an operand for the multiplier or a shift code for the scaling shifter.
Timer	TIM (15–0)	A 16-bit memory-mapped timer (counter) for timing control.

MEMORY

Memory Organization

The on-chip data RAM has 544x16-bit words, with 288 words dedicated only to data memory and the remaining 256 words configurable as either program or data memory.

- 4K words of maskable program ROM

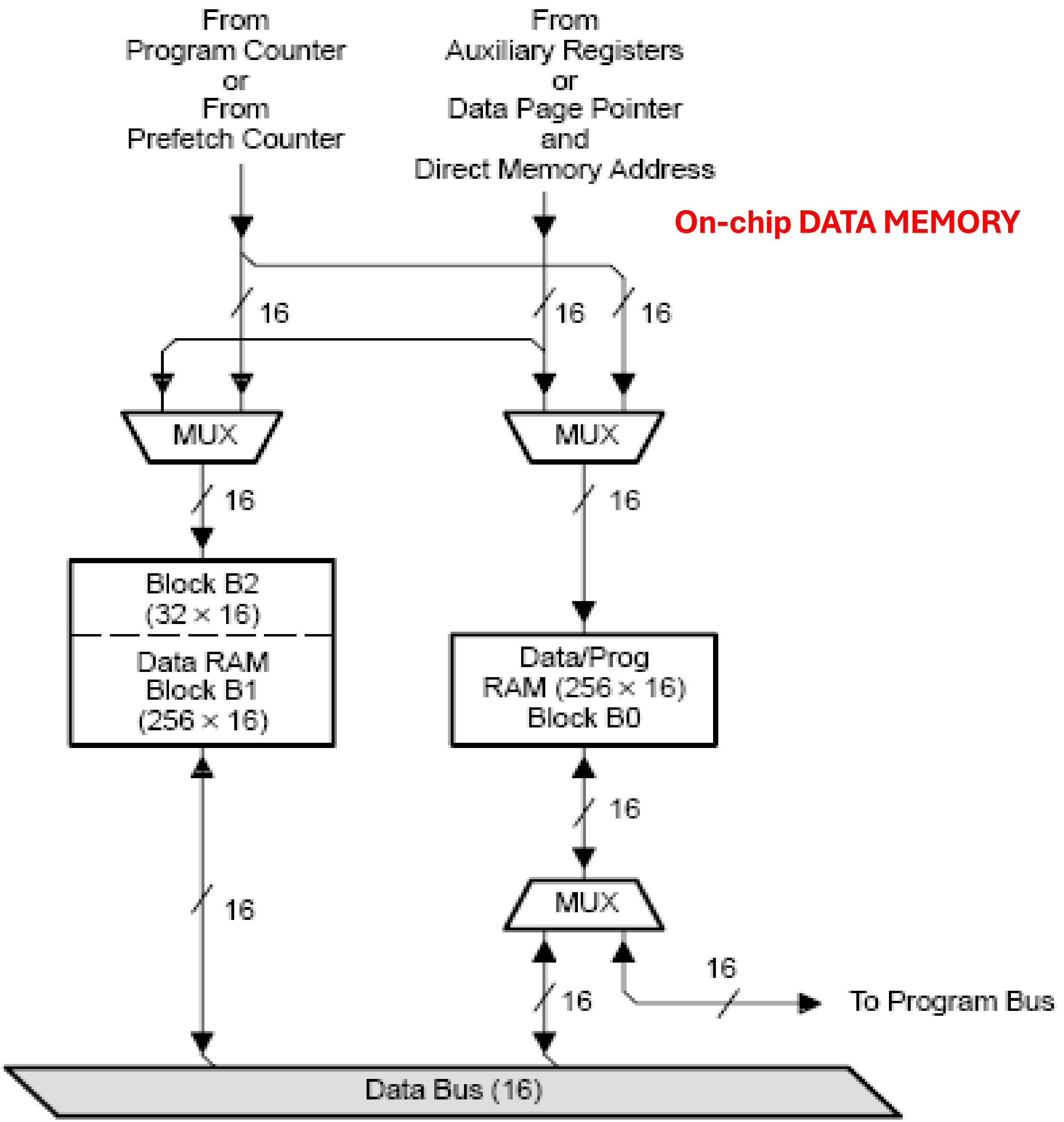
Data Memory

The 544 words of on-chip data RAM are split into three separate blocks (B0,B1, and B2) and are mapped into the lower 1Kwords of the data memory space

-TMS320C2x can address 64K words of data memory

Program Memory

-64Kwords of memory space is available. Internal RAM block B0 may be configured as program memory using instructions for that purpose (CNFD, CNFP)



TMS320C25 — Memory Map

Program Space · Data Space · I/O Space · Harvard Dual-Bus

PROGRAM MEMORY 64K × 16-bit (0x0000–0xFFFF)	
`0x0000–0x0FFF`	On-chip ROM (4K) (MP/MC = 0)
`0x0000–0x0FFF`	External Program (MP/MC = 1)
`0x1000–0xEFFF`	External Program Memory (60K words)
`0xF000–0xFFFF`	RAM B0 (CNFP) or External (CNFD) 256 words

B0 configured as program with CNFP.
MP/MC=0 maps on-chip ROM to lower 4K.

DATA MEMORY 64K × 16-bit (0x0000–0xFFFF)	
`0x0000–0x005F`	Memory-Mapped Registers DRR DXR TIM PRD IMR GREG
`0x0060–0x007F`	RAM Block B2 32 × 16-bit (data only)
`0x0080–0x00FF`	Reserved
`0x0100–0x02FF`	RAM Block B0 256 × 16-bit (when CNFD)
`0x0300–0x03FF`	RAM Block B1 256 × 16-bit (data only)
`0x0400–0x07FF`	Reserved
`0x0800–0xFFFF`	External Data Memory 63.5K × 16-bit

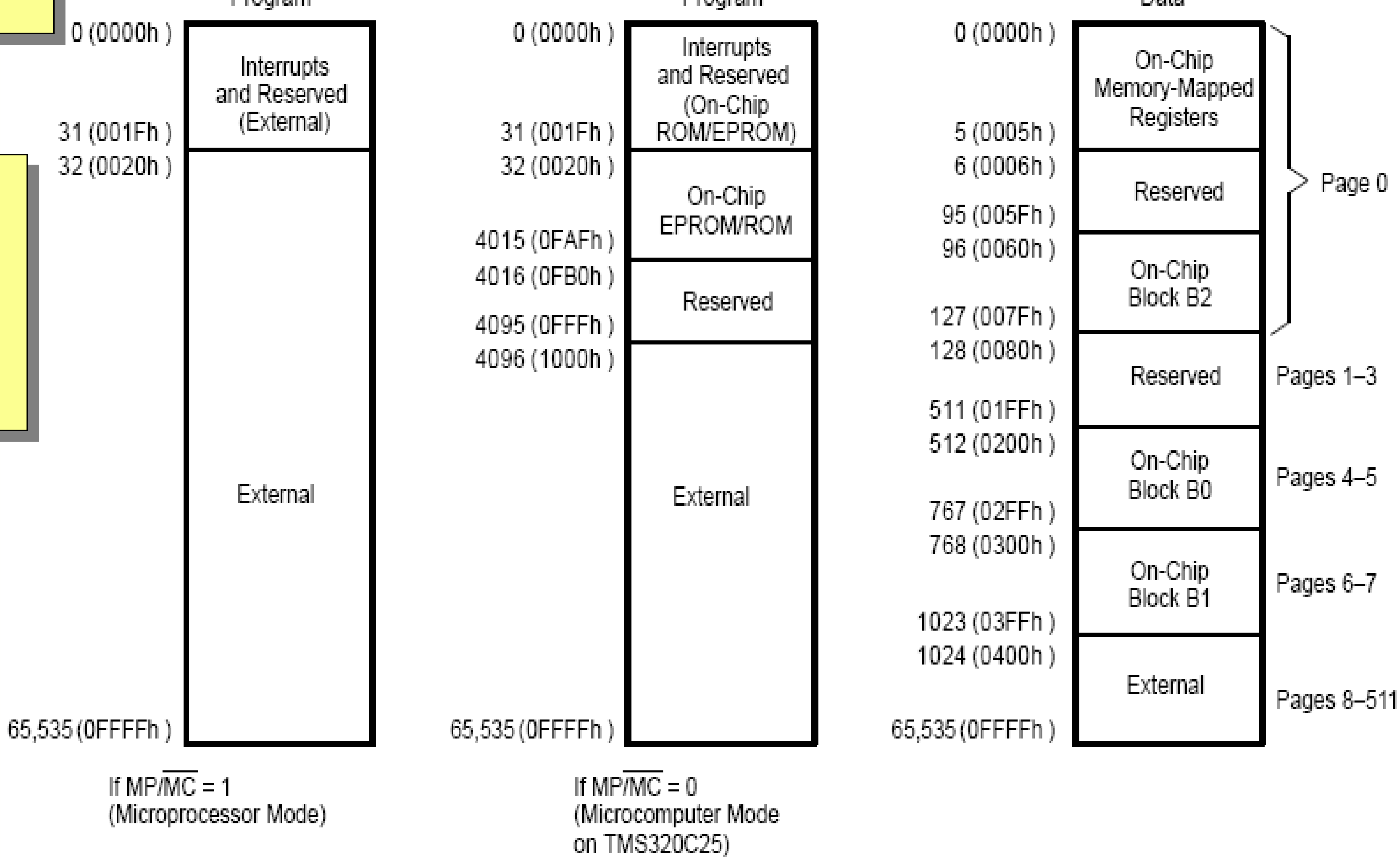
I/O SPACE 64K × 16-bit (0x0000–0xFFFF)	
`IN port#`	Input Ports (0–0xFFFF) IN Daddr, port# Reads external device
`OUT port#`	Output Ports (0–0xFFFF) OUT Daddr, port# Writes external device

Key Architecture Facts

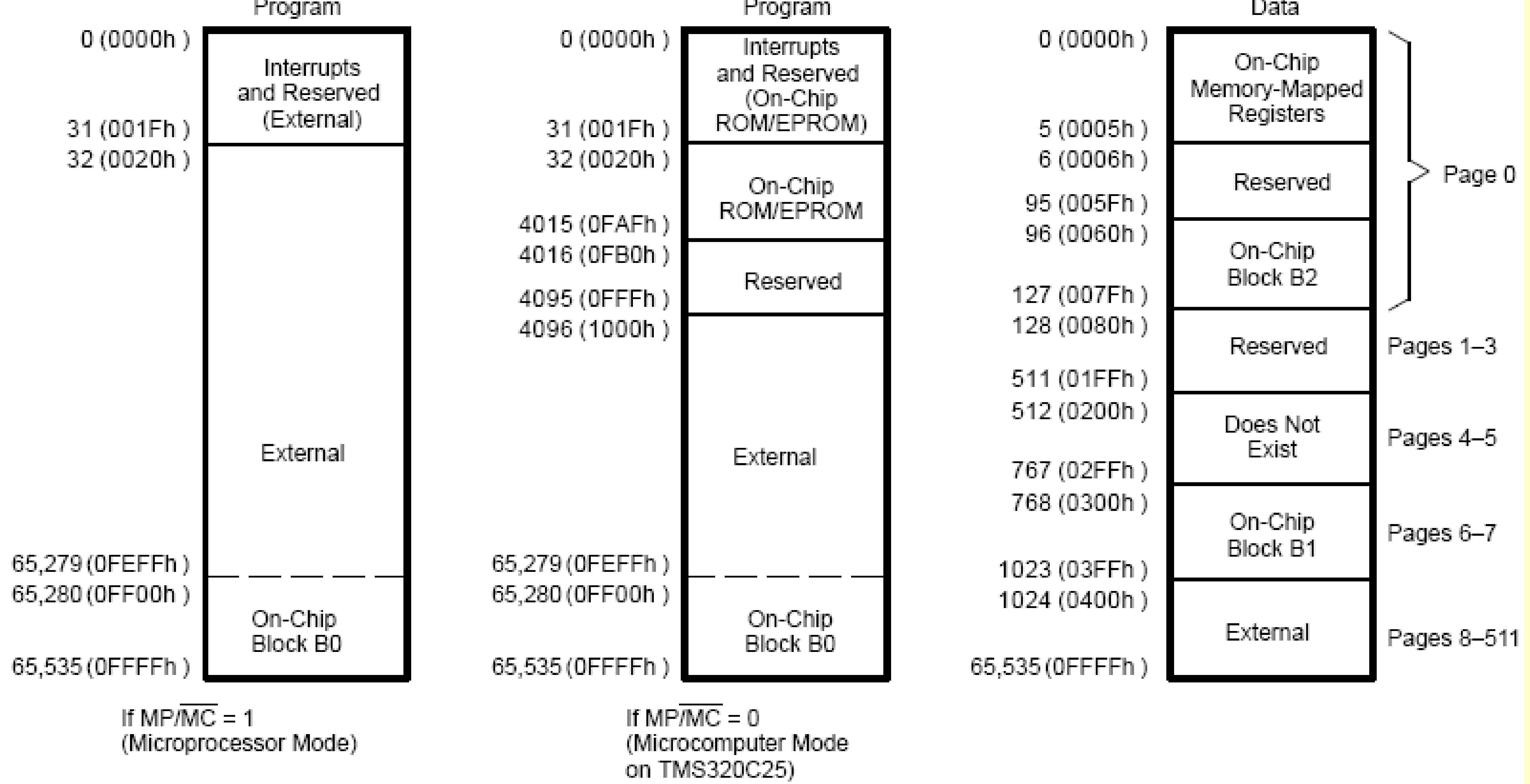
- 3 spaces: Program, Data, I/O — selected by PS, DS, $\overline{\text{IS}}$ pins
- Harvard: program fetch + data access simultaneously
- Direct addr: DP(9)+7-bit offset → 16-bit data address
- Indirect: 8 Aux Regs via ARAU (+AR0, −AR0, ±1, bit-reversed)
- Block moves: BLKD BLKP TBLR / TBLW instructions
- GREG: global memory allocation for multiprocessor designs

the PS, DS, and IS

The on-chip program ROM can be mapped into the lower 4Kw of program memory. This ROM is enabled when MP/MC =0

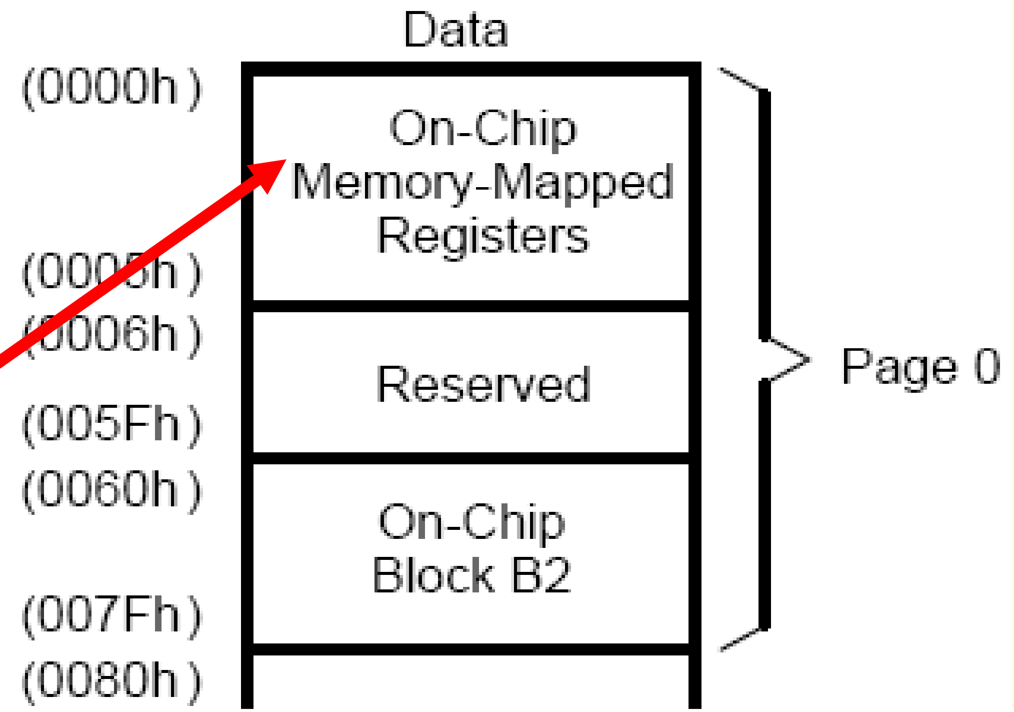


TMS320C2x Memory Maps



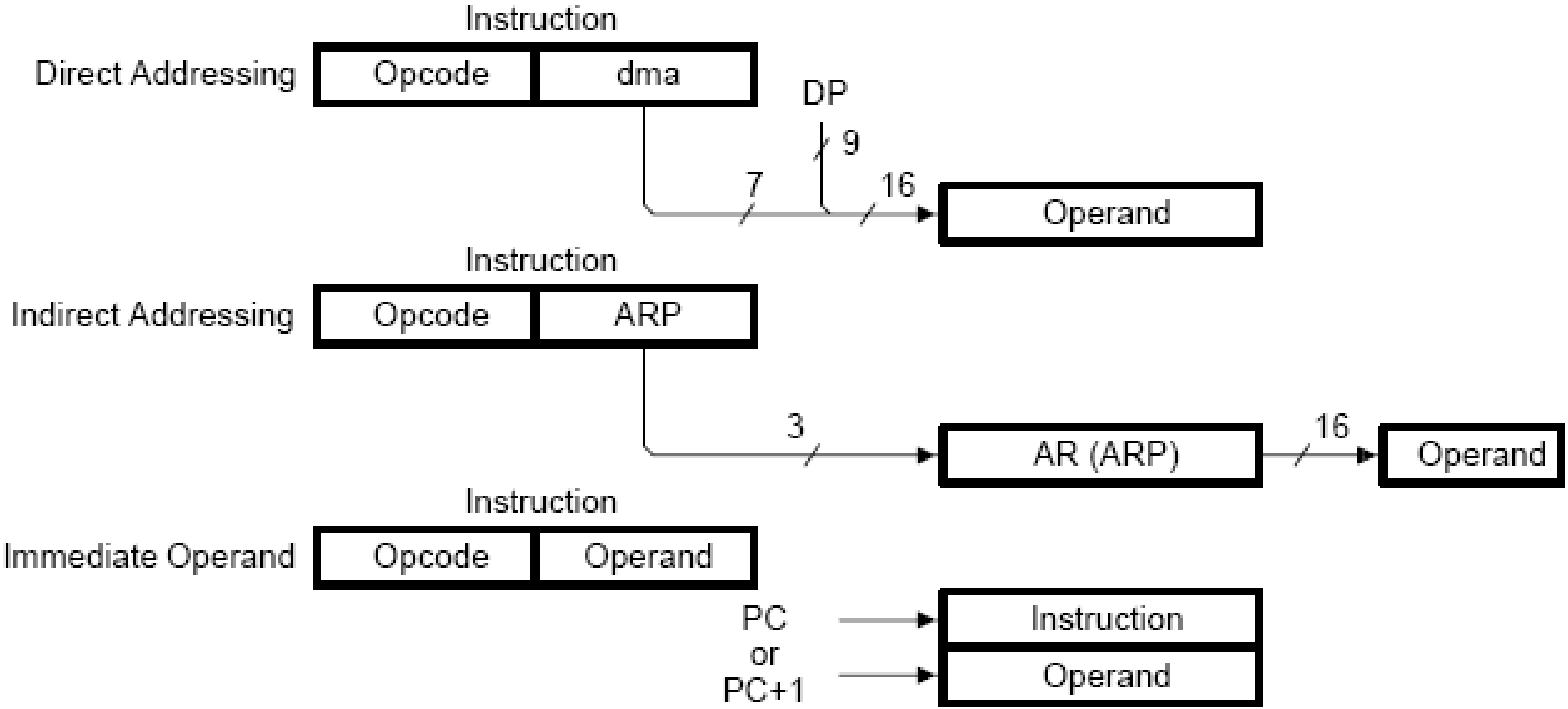
TMS320C2x Memory Maps

Memory- Mapped Registers

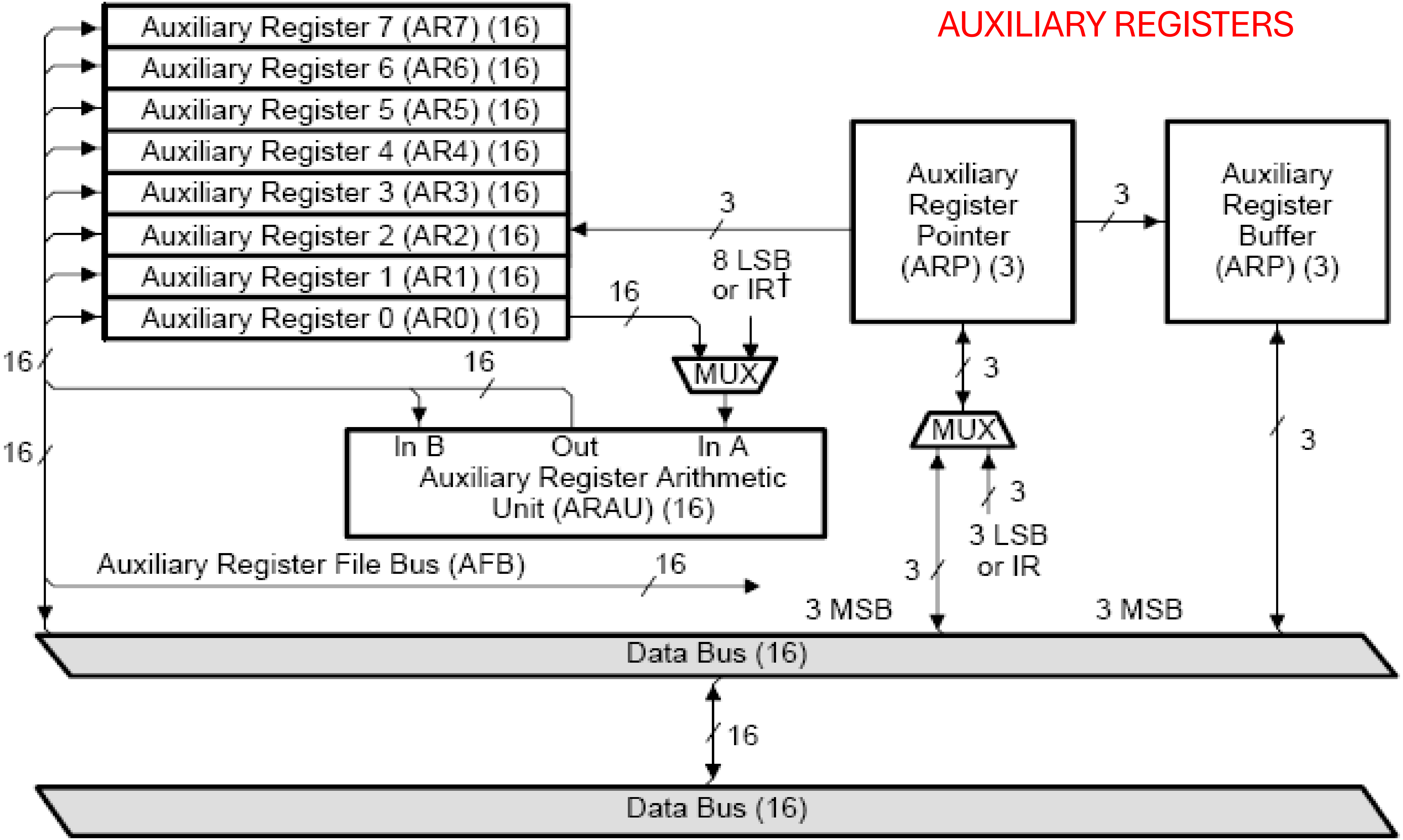


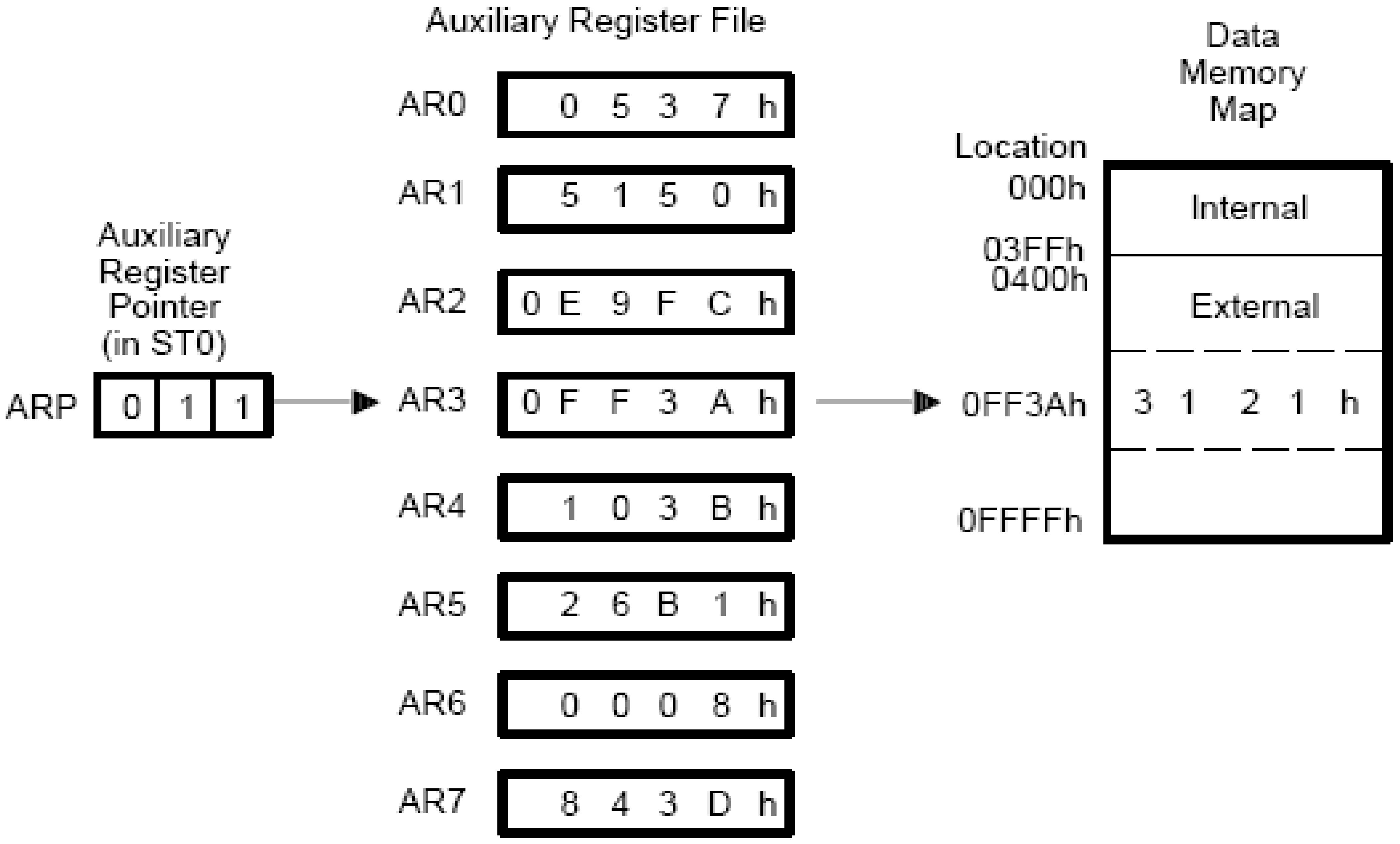
Register Name	Address Location	Definition
DRR(15–0)	0	Serial port data receive register
DXR(15–0)	1	Serial port data transmit register
TIM(15–0)	2	Timer register
PRD(15–0)	3	Period register
IMR (5–0)	4	Interrupt mask register
GREG(7–0)	5	Global memory allocation register

Modes of Operand Addressing



AUXILIARY REGISTERS





Indirect Auxiliary Register Addressing Example

The *ARAU performs* the following functions:

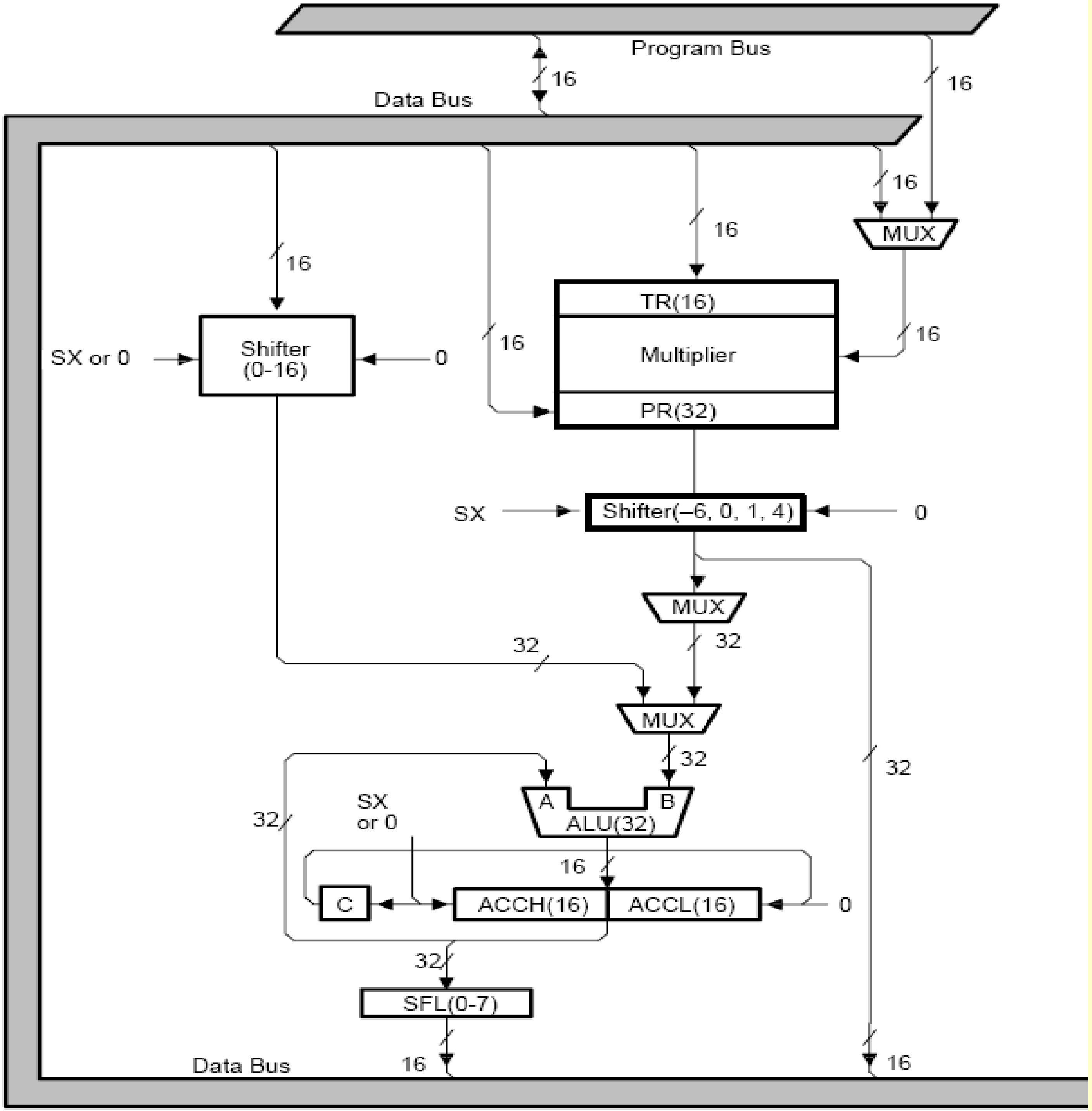
AR(ARP) + AR0 → AR(ARP)	-Index the current AR by adding a 16-bit integer contained in AR0.
AR(ARP) – AR0 → AR(ARP)	-Index the current AR by subtracting a 16-bit integer contained in AR0.
AR(ARP) + 1 → AR(ARP)	-Increment the current AR by one.
AR (ARP) – 1 → AR (ARP)	-Decrement the current AR by one.
AR (ARP) → AR (ARP)	-AR(ARP) is unchanged.
AR (ARP) + IR (7–0) → AR (ARP)	-Add 8-bit immediate value to the current AR.
AR (ARP) – IR (7 – 0) → AR (ARP)	-Subtract 8-bit immediate value to the current AR.
AR (ARP) + rcAR0 → AR (ARP)	-Bit-reversed indexing, add AR0 with reverse-carry (rc) propagation
AR (ARP) – rcAR0 → AR (ARP)	-Bit-reversed indexing, subtract AR0 with reverse-carry (rc) propagation

Memory-Memory Moves (Block Transfer)

- **BLKD** instruction moves a block within data memory
- **BLKP** instruction moves a block from program memory to data memory.
  - used with the repeat instructions (RPT/RPTK), the BLKD/BLKP instructions efficiently perform block moves from on/off-chip memory.
- **With DMOV,** a word is copied from RAM to the next address, and the CALU can process the original data at the same time.
  - ✓MACD (multiply and accumulate with data move)
  - ✓LTD (load T register, accumulate previous product, and move data) use the data move function.
- **TBLR/TBLW** (table read/write) allow words to be transferred *between program and data spaces.*
  - ✓ TBLR - read words from on-chip ROM or off-chip program ROM/RAM into the data RAM.
  - ✓TBLW - write words from on-chip data RAM to off-chip program RAM.

Central Arithmetic Logic Unit (CALU)

- Scaling Shifter
- ALU and accumulator
- Multiplier; T and P registers



Examples of TMS320C25 Carry Bit Operation

C	MSB							LSB	
X	F	F	F	F	F	F	F	F	ACC
+								1	
1	0	0	0	0	0	0	0	0	
X	7	F	F	F	F	F	F	F	ACC (OVM=0)
+								1	
0	8	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	ACC (ADD Instruction)
+								0	
0	0	0	0	0	0	0	0	1	

C	MSB							LSB	
X	0	0	0	0	0	0	0	0	ACC
–								1	
0	F	F	F	F	F	F	F	F	
X	8	0	0	0	0	0	0	0	ACC (OVM=0)
–								1	
1	7	F	F	F	F	F	F	F	
0	F	F	F	F	F	F	F	F	ACC (SUBB Instruction)
–								0	
1	F	F	F	F	F	F	F	E	

System Control : Program Counter, Stack and Related Hardware

-16-bit program counter (PC)

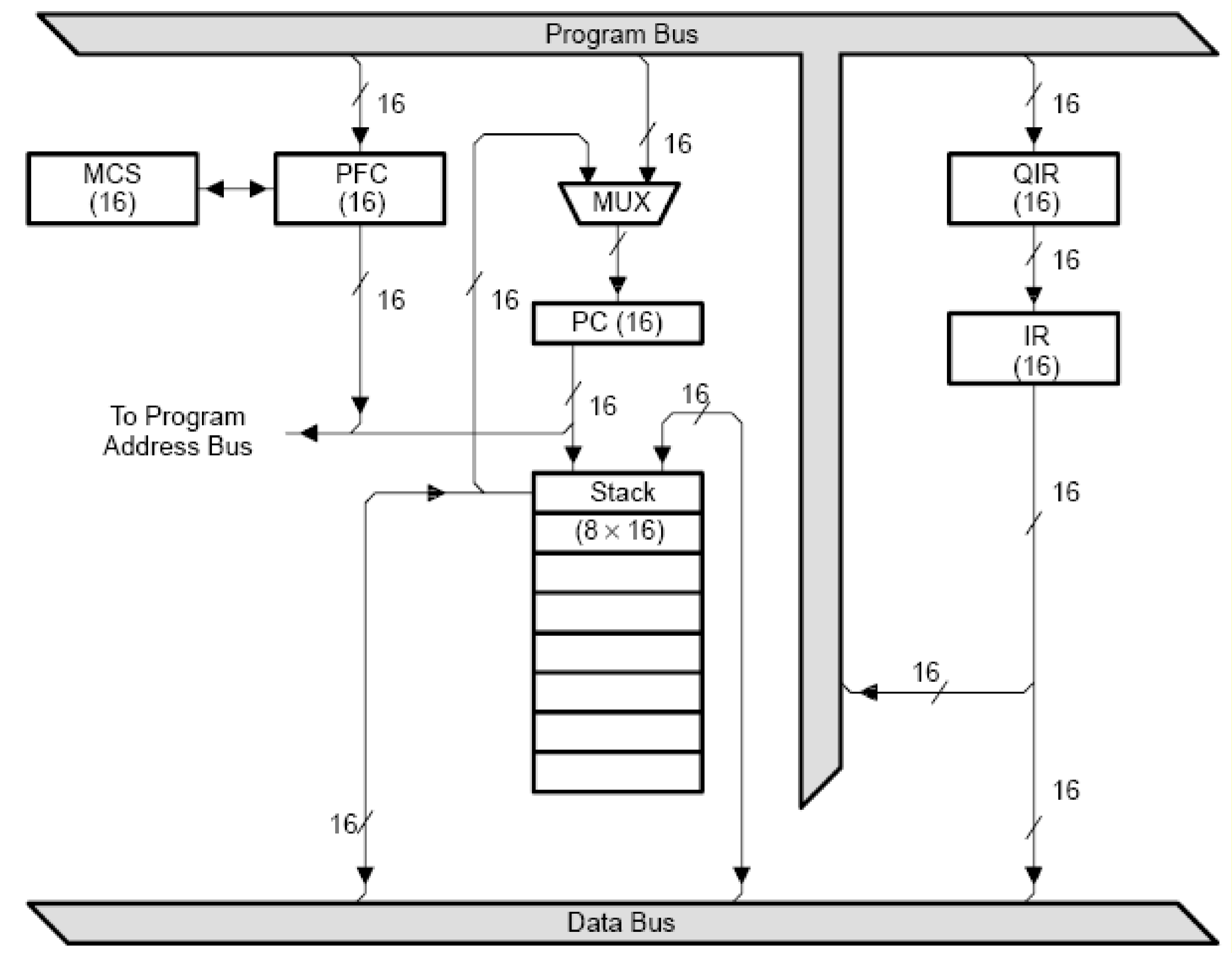
-hardware stack of 8 locations/words

- the prefetch counter (PFC)

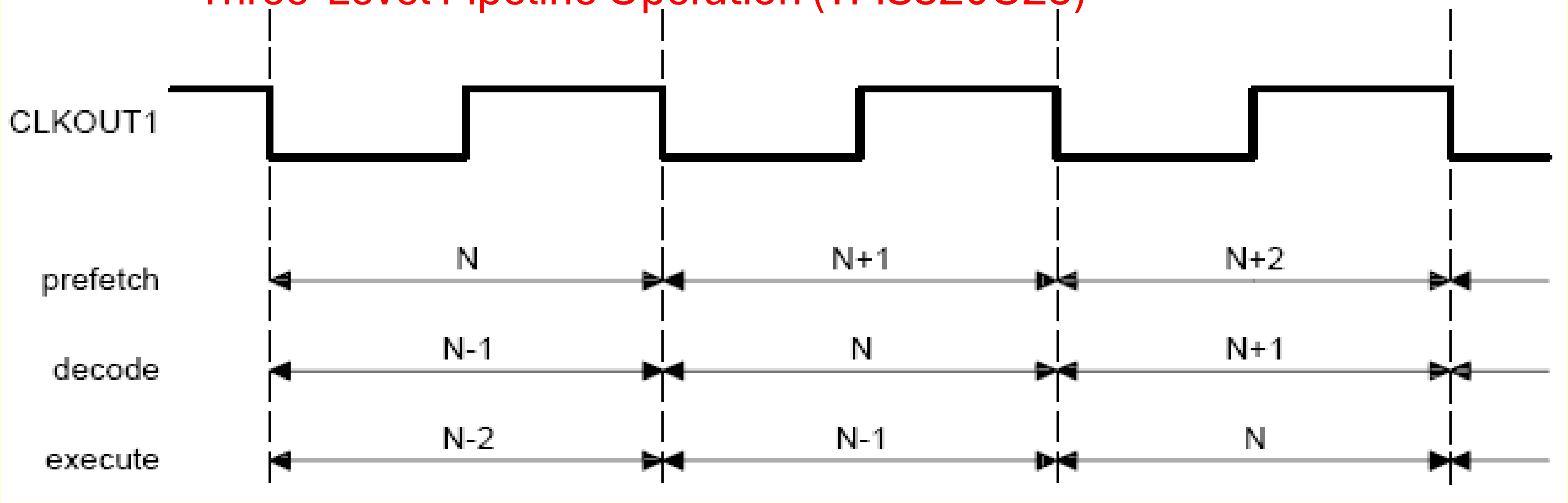
- the 16-bit micro-call-stack (MCS) register

-the instruction register (IR)

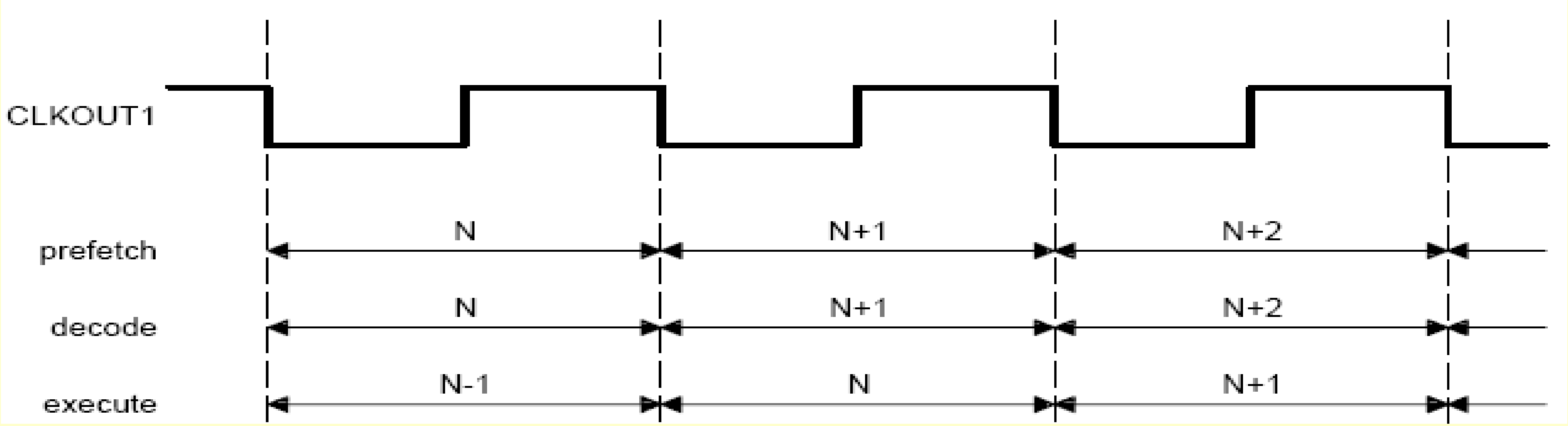
- the queue instruction register (QIR).



Three-Level Pipeline Operation (TMS320C25)



- Pipelining is reduced to two levels when execution is from internal program ROM because an instruction in internal ROM can be fetched and decoded in the same cycle.



Status Registers*

- Two status registers, ST0 and ST1, contain the status of various conditions and modes

TMS320C2x Status Register Organization

<table>
<tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>ST0</td><td colspan="3">ARP</td><td>OV</td><td>OVM</td><td>1</td><td>INTM</td><td colspan="9">DP</td></tr>
</table>

<table>
<tr><th></th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>ST1</td><td colspan="3">ARB</td><td>CNF</td><td>TC</td><td>SXM</td><td>C</td><td>1</td><td>1</td><td>HM</td><td>FSM</td><td>XF</td><td>FO</td><td>TXM</td><td colspan="2">PM</td></tr>
</table>

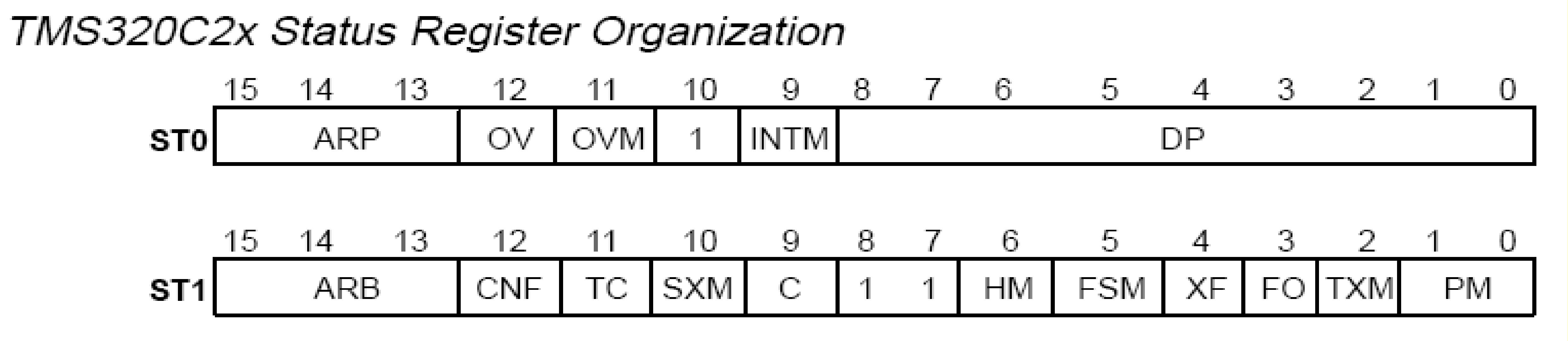
ARB - Auxiliary register pointer buffer. Whenever the ARP is loaded, the old ARP value is copied to the ARB except during an LST instruction. When the ARB is loaded via an LST1 instruction, the same value is also copied to the ARP.

ARP - Auxiliary register pointer. This three-bit field selects the AR to be used in indirect addressing. When ARP is loaded, the old ARP value is copied to the ARB register.
ARP may be modified by memory-reference instructions when using indirect addressing, and by the LARP, MAR, and LST instructions. ARP is also loaded with the same value as ARB when an LST1 instruction is executed.

C-Carry bit. C= 1 if the result of an addition generates a carry, *or C=0 if the result of a subtraction generates a borrow*. (borrow = inverted carry convention). Otherwise, C=0 after an addition and C=1 after a subtraction, except if the instruction is ADDH or SUBH. ADDH can only set, and SUBH only reset the C bit but cannot affect it otherwise. These instructions will also affect C bit: SC, RC, LST1, shift, and rotate. Two branch instructions, BC and BNC, have been provided to branch on the status of C. C = 1 on a reset.

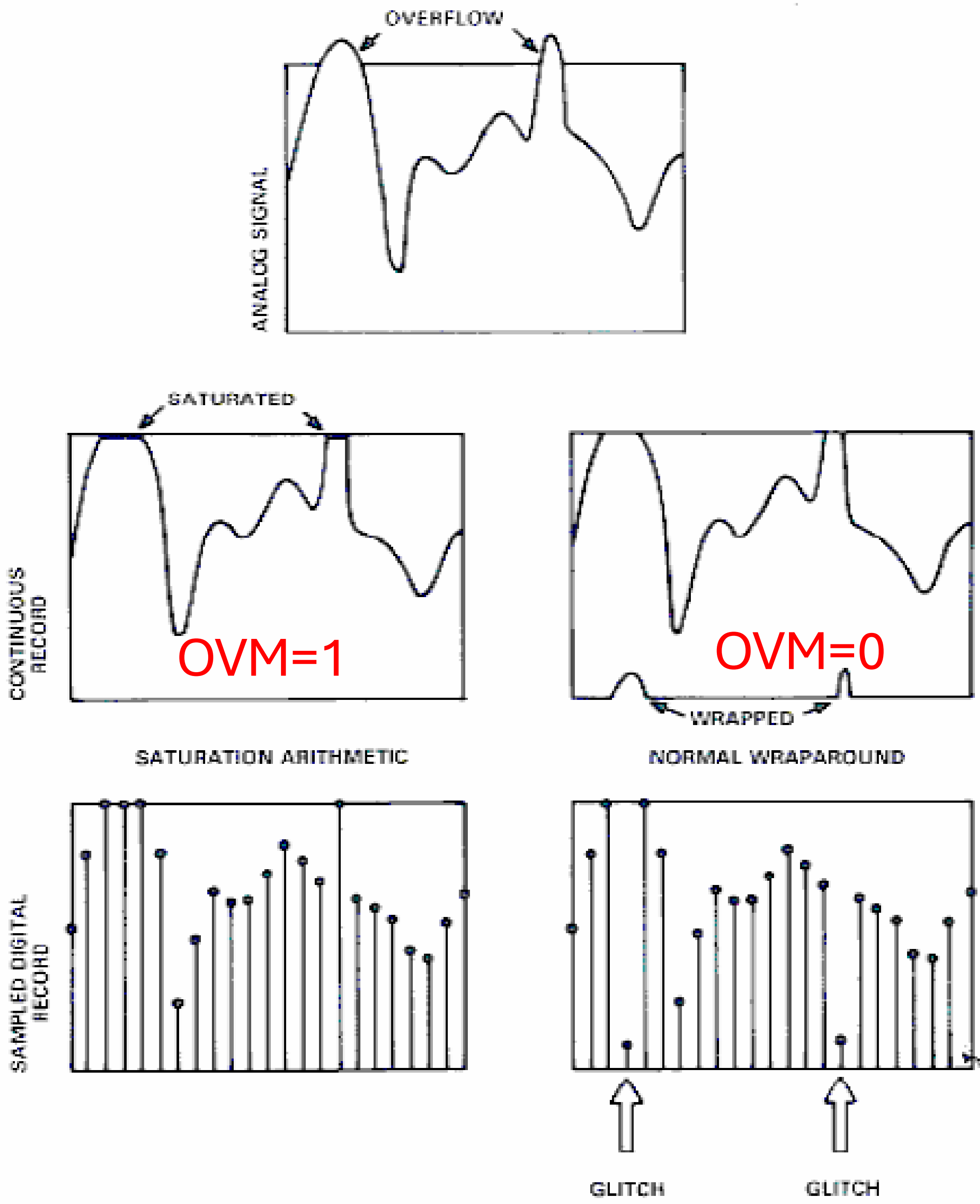
OV Overflow flag bit. As a latched overflow signal, OV=1 when overflow occurs in the ALU. Once an overflow occurs, the OV remains set until a: reset, BV, BNV, or LST instruction clears the OV.

OVM Overflow mode bit. When OVM=0, overflowed result overflows normally in the ACC. When OVM=1, the accumulator is set to either its most positive or its most negative value upon encountering an overflow. The SOVM and ROVM instructions set and reset this bit, respectively. LST may also be used to modify the OVM.



8-Bit ALU Operation (Without Saturation)

	10110111	(−73)	−73
	+ 11001101	(−51)	+ −51
	10000100	(−124)	−124
	+ 11010011	(−45)	+ −45
Rollover →	01010111	(57)	−169
	+ 00111011	(59)	+ 59
	10010010	(−110)	−110



CNF On-chip RAM configuration control bit. If CNF=0, block B0 is configured as data memory; otherwise, block B0 is configured as program memory. The CNF may be modified by the CNFD, CNFP, and LST1 instructions. After reset the CNF=0.

DP Data memory page pointer. Concatenating the 9-bit DP register with the 7 LSBs of an instruction word forms a 16-bit direct memory address. DP may be changed by the LST, LDP, and LDPK instructions.

FO Format bit. When FO=0, the serial port registers configure themselves as 16-bit registers. When FO=1, the port registers are configured to receive and transmit 8-bit characters. FO may be modified by the FORT and LST1 instructions. FO=0 after reset.

FSM Frame synchronization mode bit. This bit indicates whether the serial port operates with/without frame sync pulses. When FSM = 1, the serial port operation is initiated following a frame sync pulse on the FSX/FSR inputs. When FSM = 0, the FSX/FSR inputs are ignored and the serial port operates continuously with no frame sync pulses required. The FO =1 after a reset.

TMS320C2x Status Register Organization

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST0	ARP			OV	OVM	1	INTM	DP								

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	ARB			CNF	TC	SXM	C	1	1	HM	FSM	XF	FO	TXM	PM	

HM Hold mode bit. When HM = 1, the processor halts internal execution when acknowledging an active HOLD. When HM = 0, the processor may continue execution out of internal program memory but puts its external interface in a high-impedance state. This bit is set to 1 by a reset.

INTM Interrupt mode bit. When INTM=0, all unmasked interrupts are enabled. When set to 1, all maskable interrupts are disabled. INTM is set/reset by the DINT and EINT instructions. RS and IACK also set INTM. INTM has no effect on the unmaskable RS interrupt. Note that INTM is unaffected by the LST instruction.

PM Product shift mode. If these two bits are:
PM= 00, the multiplier's 32-bit product is sent to the ALU with no shift.
PM = 01, the PR output is left-shifted 1 bit and loaded into the ALU, with the LSBs zero-filled.
PM = 10, the PR output is left-shifted by 4 bits and loaded into the ALU, with the LSBs zero-filled.
PM = 11 produces a right shift of 6 bits, sign-extended. PR contents remain unchanged.
The shift takes place when transferring the contents of the PR to the ALU.
PM is loaded by the SPM or LST1 instructions. The PM bits are cleared by RS.

TMS320C2x Status Register Organization

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST0	ARP			OV	OVM	1	INTM	DP								

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1	ARB			CNF	TC	SXM	C	1	1	HM	FSM	XF	FO	TXM	PM	

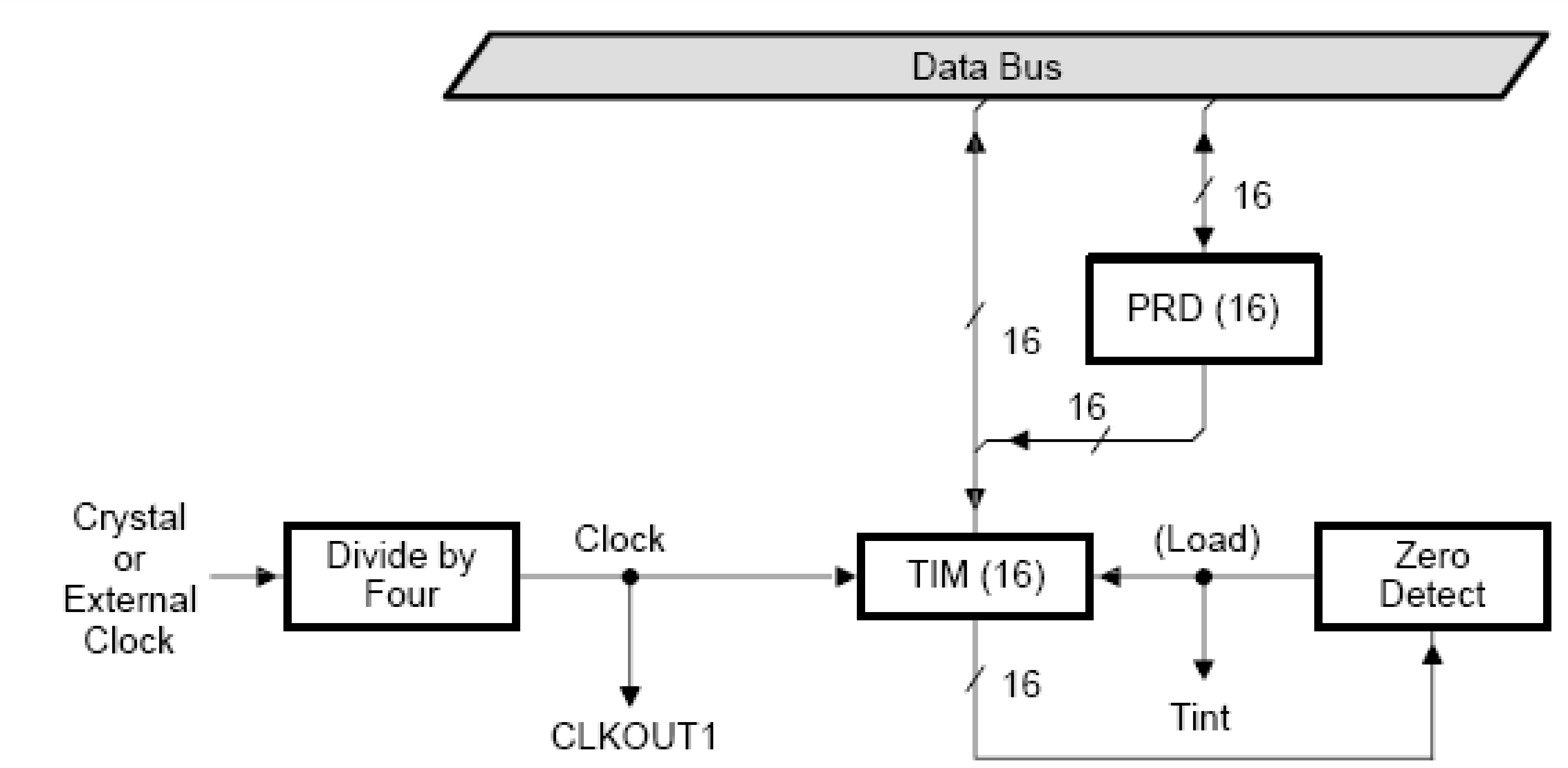
SXM Sign-extension mode bit. SXM = 1 produces sign extension on data as it is passed into the accumulator through the scaling shifter. SXM = 0 suppresses sign extension. SXM does not affect the definition of certain instructions; for example, the ADDS instruction suppresses sign extension regardless of SXM. This bit is set and reset by the SSXM and RSXM instructions and may also be loaded by LST1. SXM =1 after Reset.

TC Test/control flag bit. The TC bit is affected by the BIT, BITT, CMPR, LST1, and NORM instructions. The TC =1 if a bit tested by BIT or BITT is a 1, if a compare condition tested by CMPR exists between AR0 and another AR pointed to by ARP, or if the exclusive-OR function of the two MSBs of the accumulator is true when tested by a NORM instruction. Two branch instructions, BBZ and BBNZ, provide branching on the status of the TC.

TXM Transmit mode bit.
TXM = 1 *configures the serial port's FSX pin* to be an output. In this mode, a pulse is produced on FSX when DXR is loaded. Transmission then starts on the DX pin.
TXM = 0 *configures the FSX pin* to be an input. TXM is set and reset by the STXM and RTXM instructions and may also be loaded by LST1. Reset put TXM=0.

XF - XF pin status bit. This status bit indicates the state of the XF pin, a general-purpose output pin. XF is set and reset by the SXF and RXF instructions or may be loaded by LST1. XF is set to 1 by RS.

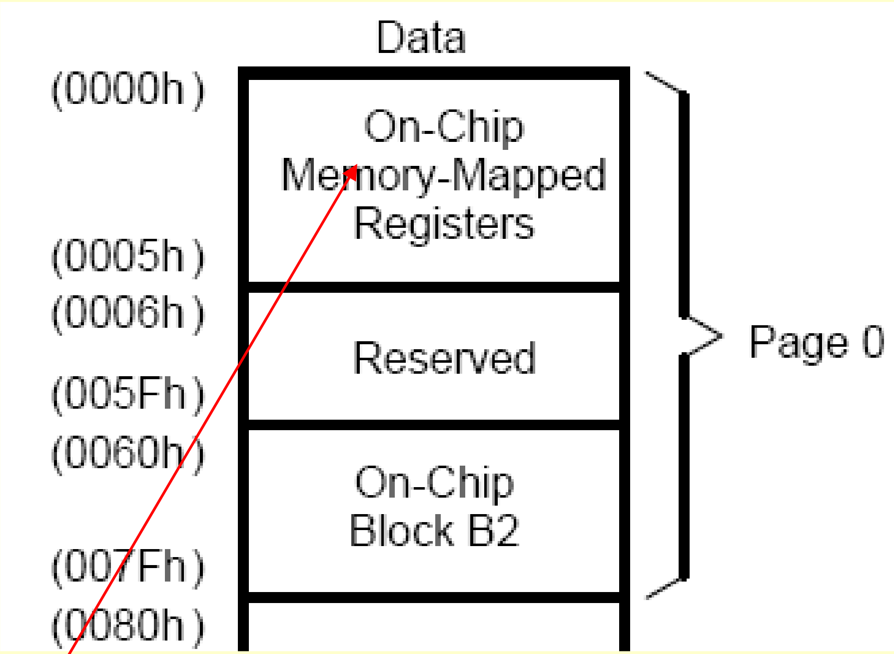
Peripherals



$$F_S = F_{int} = F_{CLKOUT1}/(PRD+1))$$

Timer programming

```
FCLK    equ     20000 ; kHz
Fs      equ     20          ;sampling frequency kHz
prd     equ     FCLK/(4*Fs) -1   ;prd=124
..................
LALK    prd                 ; Accl=PRD
SACL    3                   ;PRD= Accl
```

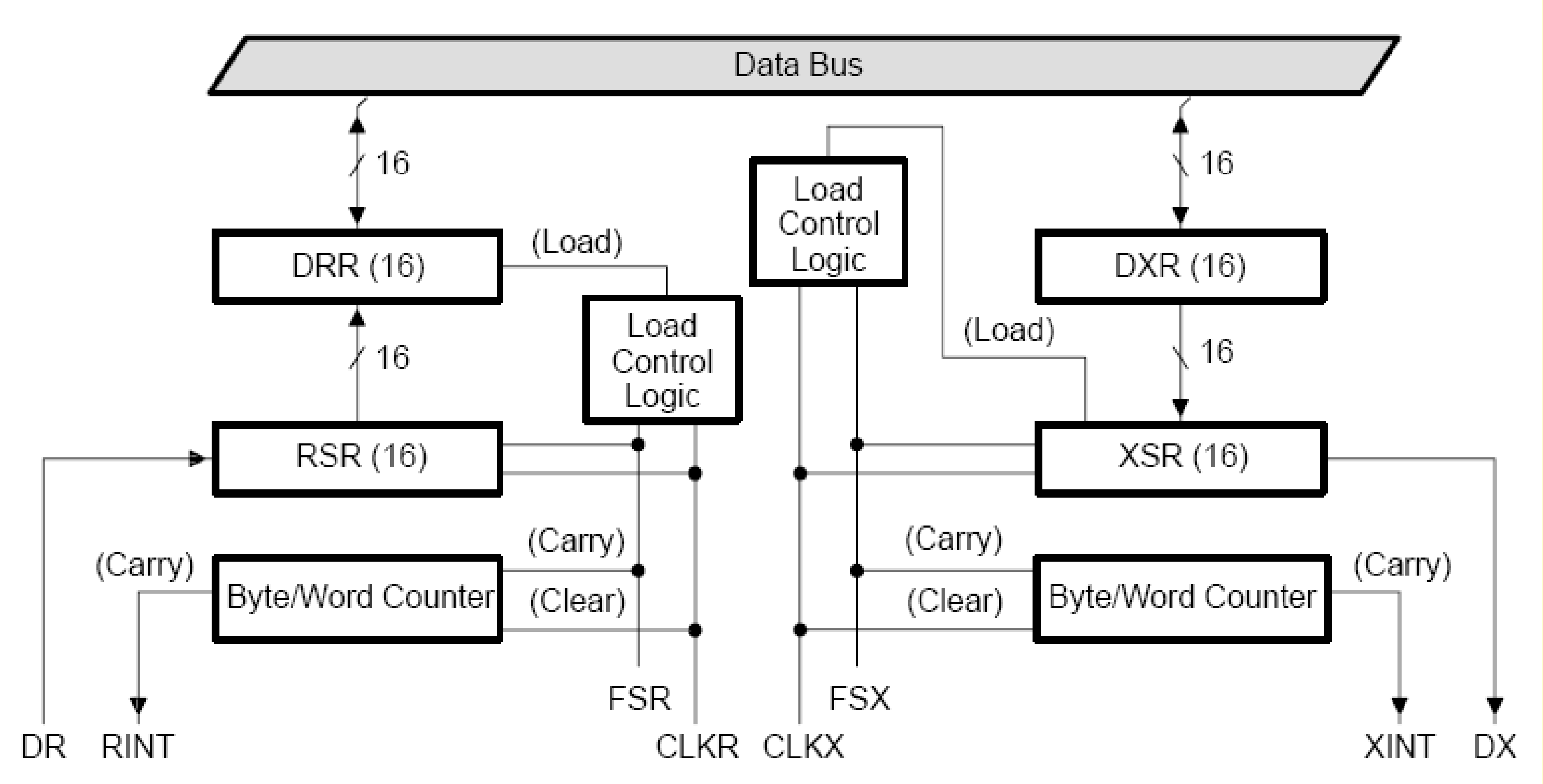


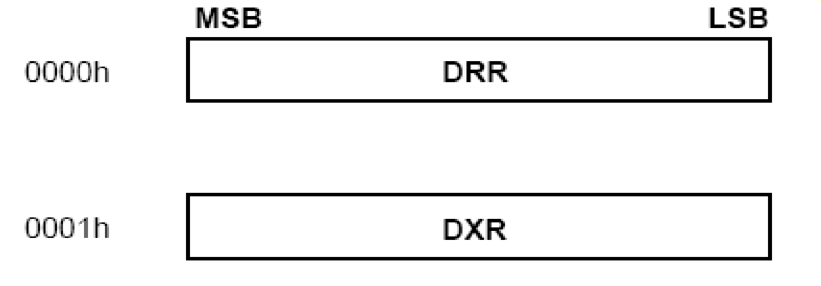
Register Name	Address Location	Definition
DRR(15–0)	0	Serial port data receive register
DXR(15–0)	1	Serial port data transmit register
TIM(15–0)	2	Timer register
PRD(15–0)	3	Period register
IMR (5–0)	4	Interrupt mask register
GREG(7–0)	5	Global memory allocation register

SERIAL PORT

• A full-duplex on-chip serial port provides direct communication with serial devices such as codecs, serial A/D converters, and other serial systems

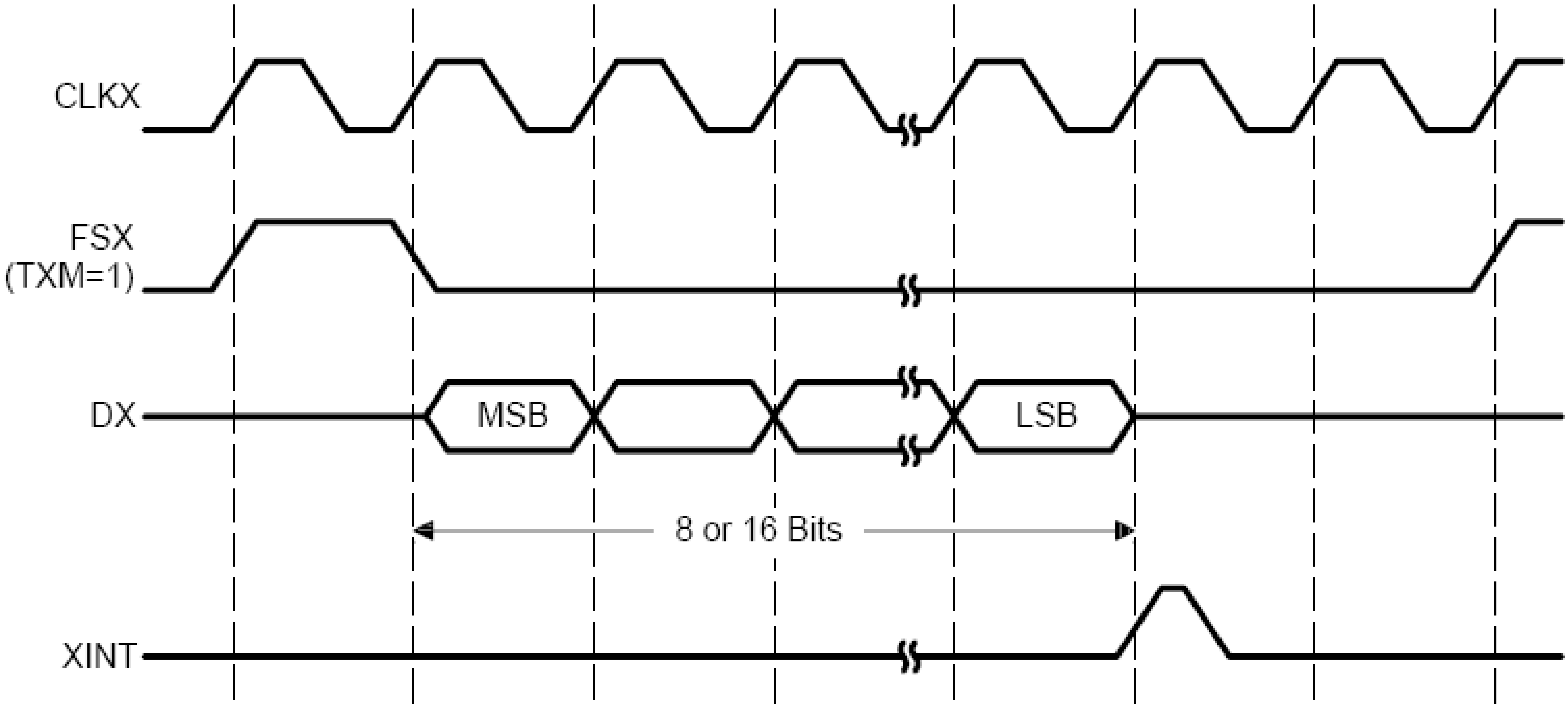
Serial Port Bits/Pins/Registers	
FO	Format bit
TXM	Transmit mode bit
FSM	Frame synchronization mode bit
CLKX	Transmit clock signal
CLKR	Receive clock signal
DX	Transmitted serial data signal
DR	Received serial data signal
FSX	Transmit framing synchronization signal
FSR	Receive framing synchronization signal
DXR	Data transmit register
DRR	Data receive register
XSR	Transmit shift register
RSR	Receive shift register



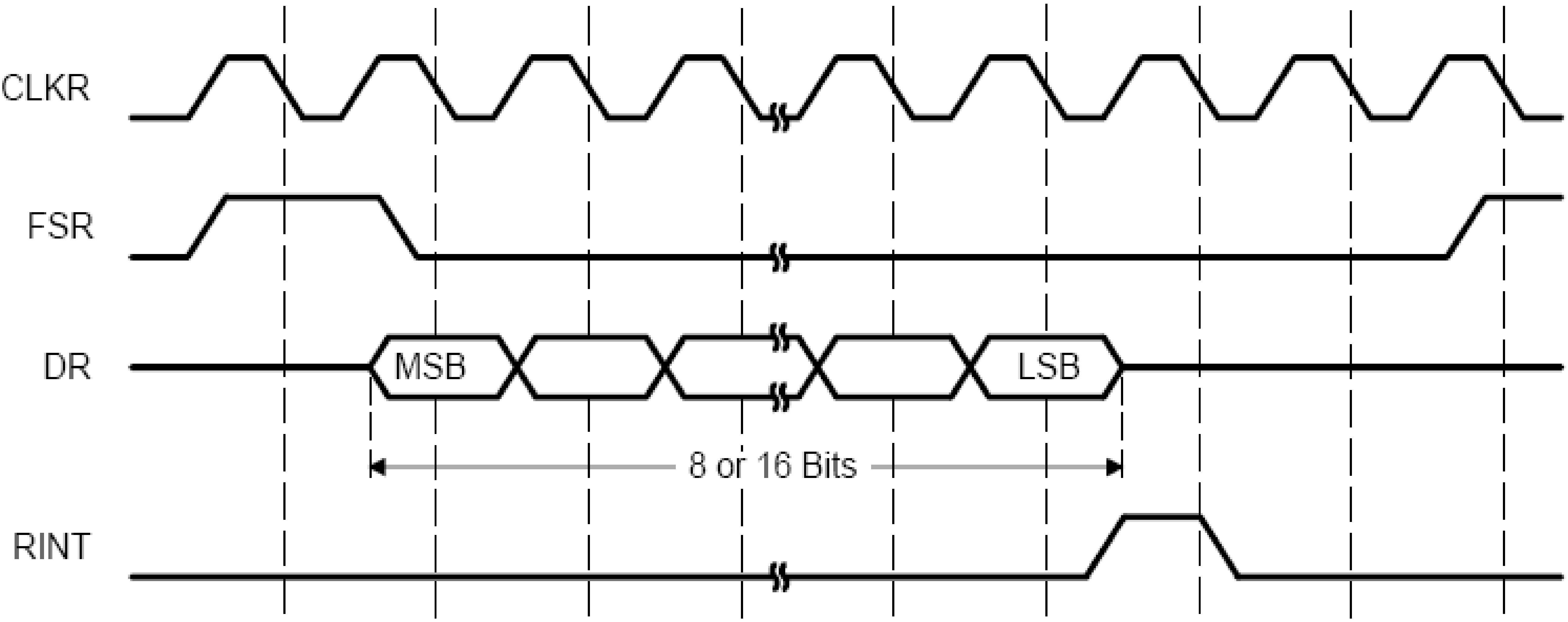


SERIAL PORT BLOCK DIAGRAM

Serial Port Transmit Timing Diagram



Serial Port Receive Timing Diagram



INTERRUPTS

Interrupt Name	Memory Location	Priority	Function
$\overline{\text{RS}}$	0h	1 (highest)	External reset signal
$\overline{\text{INT0}}$	1h	2	External user interrupt #0
$\overline{\text{INT1}}$	2h	3	External user interrupt #1
$\overline{\text{INT2}}$	3h	4	External user interrupt #2
	8–17h		Reserved locations
TINT	18h	5	Internal timer interrupt
RINT	1Ah	6	Serial port receive interrupt
XINT	1Ch	7 (lowest)	Serial port transmit interrupt
TRAP	1Eh	N/A	TRAP instruction address

Ex. Using IMR to mask TINT:

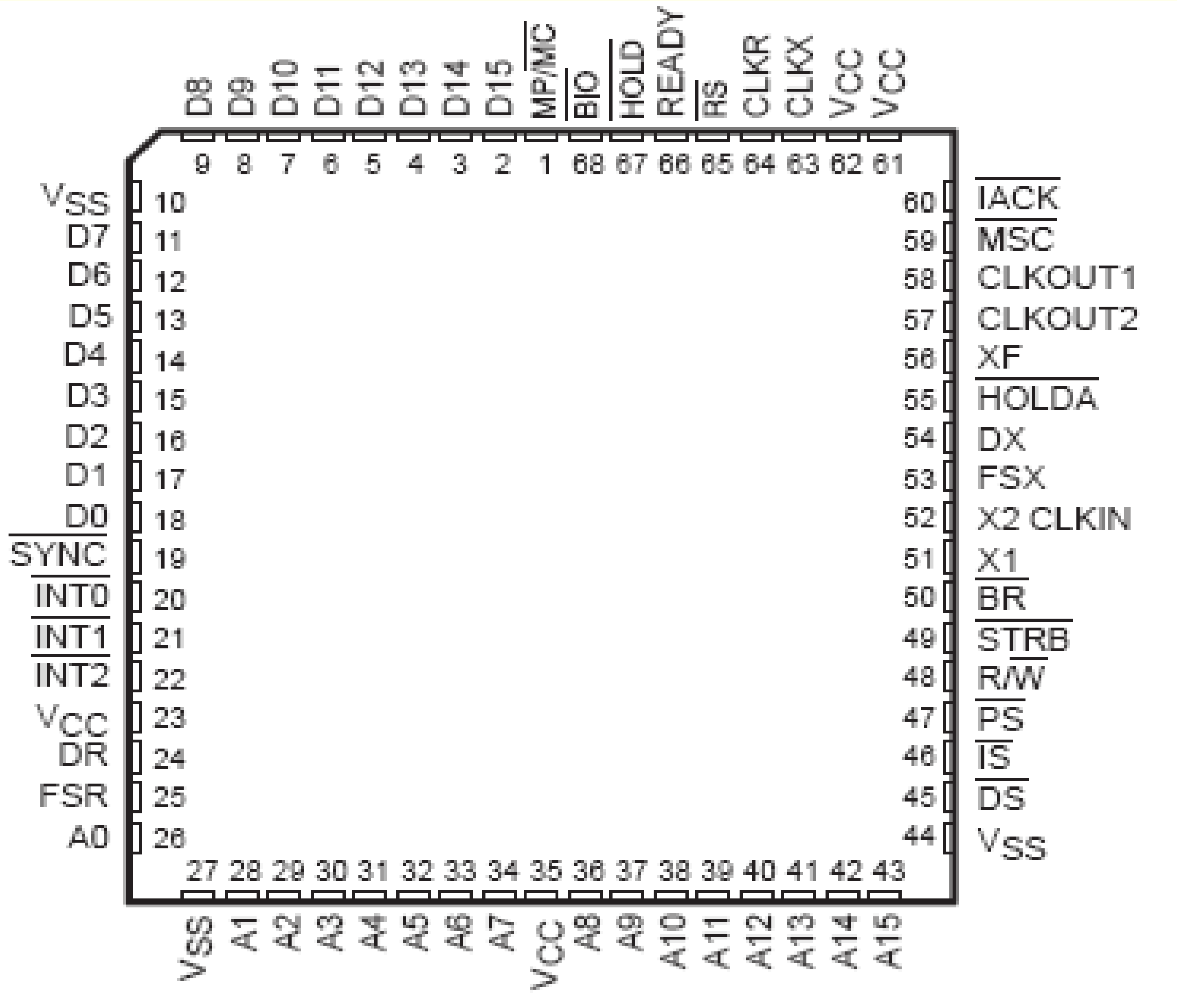
```
LALK  8        ; interrupt mask for TINT Accl=0008h
OR 4           ; ACC=ACC U (IMR)
SACL 4         ; (IMR) =Accl
EINT
```

Interrupt Mask Register (IMR)

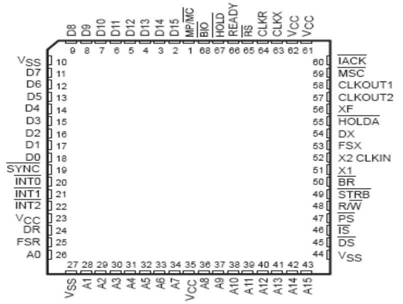
15–6	5	4	3	2	1	0
RESERVED	XINT	RINT	TINT	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$

Register Name	Address Location	Definition
DRR(15–0)	0	Serial port data receive register
DXR(15–0)	1	Serial port data transmit register
TIM(15–0)	2	Timer register
PRD(15–0)	3	Period register
IMR (5–0)	4	Interrupt mask register
GREG(7–0)	5	Global memory allocation register

TMS320C2x Signal Descriptions



SIGNALS	I/O/Z‡	DEFINITION
V_{CC}	I	5-V supply pins
V_{SS}	I	Ground pins
X1	O	Output from internal oscillator for crystal
X2/CLKIN	I	Input to internal oscillator from crystal or external clock
CLKOUT1	O	Master clock output (crystal or CLKIN frequency/4)
CLKOUT2	O	A second clock output signal
D15-D0	I/O/Z	16-bit data bus D15 (MSB) through D0 (LSB). Multiplexed between program, data, and I/O spaces.
A15-A0	O/Z	16-bit address bus A15 (MSB) through A0 (LSB)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select signals
R/$\overline{W}$	O/Z	Read/write signal
$\overline{STRB}$	O/Z	Strobe signal
$\overline{RS}$	I	Reset input
$\overline{INT2}$-$\overline{INT0}$	I	External user interrupt inputs
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select pin
$\overline{MSC}$	O	Microstate complete signal
$\overline{IACK}$	O	Interrupt acknowledge signal
READY	I	Data ready input. Asserted by external logic when using slower devices to indicate that the current bus transaction is complete.
$\overline{BR}$	O	Bus request signal. Asserted when the TMS320C2x requires access to an external global data memory space.
XF	O	External flag output (latched software-programmable signal)
$\overline{HOLD}$	I	Hold input. When asserted, TMS320C2x goes into an idle mode and places the data, address, and control lines in the high impedance state.
$\overline{HOLDA}$	O	Hold acknowledge signal
$\overline{SYNC}$	I	Synchronization input
$\overline{BIO}$	I	Branch control input. Polled by BIOZ instruction.
DR	I	Serial data receive input
CLKR	I	Clock for receive input for serial port
FSR	I	Frame synchronization pulse for receive input
DX	O/Z	Serial data transmit output
CLKX	I	Clock for transmit output for serial port
FSX	I/O/Z	Frame synchronization pulse for transmit. Configuration as either an input or an output.



‡ I/O/Z denotes input/output/high-impedance state.

Address/Data Buses

A15-A0 (O/TS)-Parallel address bus A15 (MSB) through A0 (LSB). Multiplexed to address external data/program memory or I/O. Placed in high-impedance state in the hold mode.

D15-D0 (I/O/TS)-Parallel data bus D15 (MSB) through D0 (LSB). Multiplexed to transfer data between the TMS320C2x and external data/program memory or I/O devices. Placed in the high-impedance state when not outputting or when RS or HOLD is asserted.

Interface Control Signals

/DS, /PS, /IS (O/TS) Data, program, and I/O space select signals. Always high unless low level asserted for communicating to a particular external space. Placed in high-impedance state in the hold mode.

READY (I) Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY = 0), the TMS320C2x waits one cycle and checks READY again. READY also indicates a bus grant to an external device after a BR (bus request) signal.

R/ /W (O/TS) Read/write signal. Indicates transfer direction when communicating to an external device. Normally in read mode (high), unless low level asserted for performing a write operation. Placed in high-impedance state in the hold mode.

/STRB (O/TS) Strobe signal. Always high unless asserted low to indicate an *external bus cycle*. Placed in high-impedance state in the hold mode.

Multiprocessing Signals

BR **(O)** Bus request signal. Asserted when the TMS320C2x requires access to an **external global data memory space**. READY is asserted to the device when the bus is available, and the global data memory is available for the bus transaction.

HOLD **(I)** Hold input. When this signal is asserted, the TMS320C2x places the data, address, and control lines in the *high-impedance state*.

HOLDA **(O)** Hold acknowledge signal. Indicates that the TMS320C2x has gone into the hold mode and that an external processor may access the local external memory of the TMS320C2x.

SYNC **(I)** Synchronization input. Allows clock synchronization of two or more TMS320C2xs. SYNC is an active-low signal and must be asserted on the rising edge of CLKIN.

Interrupt and Miscellaneous Signals

BIO (I) Branch control input. Polled by BIOZ instruction. If BIO=0, the DSP executes a branch. This signal must be active during the BIOZ instruction fetch.

IACK (O) Interrupt acknowledge signal. Output is valid only while CLKOUT1 is low. Indicates receipt of an interrupt and that the program is branching to the interrupt-vector location designated by A15–A0.

INT2 (I) External user interrupt inputs. Prioritized and makable by the interrupt mask
INT1 register and the interrupt mode bit.
INT0

MP/$\overline{\text{MC}}$ (I) Microprocessor/microcomputer mode select pin for the TMS320C25. When asserted low (microcomputer mode), the pin causes the internal ROM t0 mapped into the lower 4K words of the program memory map. In the microprocessor mode, the lower 4K words of program memory are external.

MSC (O) Microstate complete signal. Asserted low and valid only during CLKOUT1 low when the TMS320C2x has just completed a memory operation, such as an instruction-fetch or a data memory read/write. MSC can be used to generate a **one wait-state READY** signal for slow memory.

RS (I) Reset input. Causes the TMS320C2x to terminate execution and forces the **PC=0.** When RS is brought to a high level, execution begins at location zero of program memory. RS affects various registers and status bits.

XF (O) External flag output (latched software-programmable signal). Used for signaling other processors in multiprocessor configurations or as a general- purpose output pin.

Supply/Oscillator Signals

CLKOUT1 **(O)** Master clock output signal (CLKIN frequency/4). CLKOUT1 rises at the beginning of quarter-phase 3 (Q3) and falls at the beginning of quarter-phase 1 (Q1).

CLKOUT2 **(O)** A second clock output signal. CLKOUT2 rises at the beginning of quarter-phase 2 (Q2) and falls at the beginning of quarter phase 4 (Q4).

VCC **(I)** Four 5-V supply pins, tied together externally.
VSS **(I)** Three ground pins, tied together externally.

X1 **(O)** Output pin from the internal oscillator for the crystal. If a crystal is not used, this pin should be left unconnected.
X2/CLKIN **(I)** Input pin to the internal oscillator from the crystal. If crystal is not used, a clock may be input to the device on this pin

Serial Port Signals

CLKR **(I)** Receive clock input. External clock signal for clocking data from the DR (data receive) pin into the RSR (serial port receive shift register). Must be present during serial port transfers.

CLKX **(I)** Transmit clock input. External clock signal for clocking data from the XSR (serial port transmit shift register) to the DX (data trans-mit) pin. Must be present during serial port transfers.

DR **(I)** Serial data receive input. Serial data is received in the RSR (serial port receive shift register) via the DR pin.

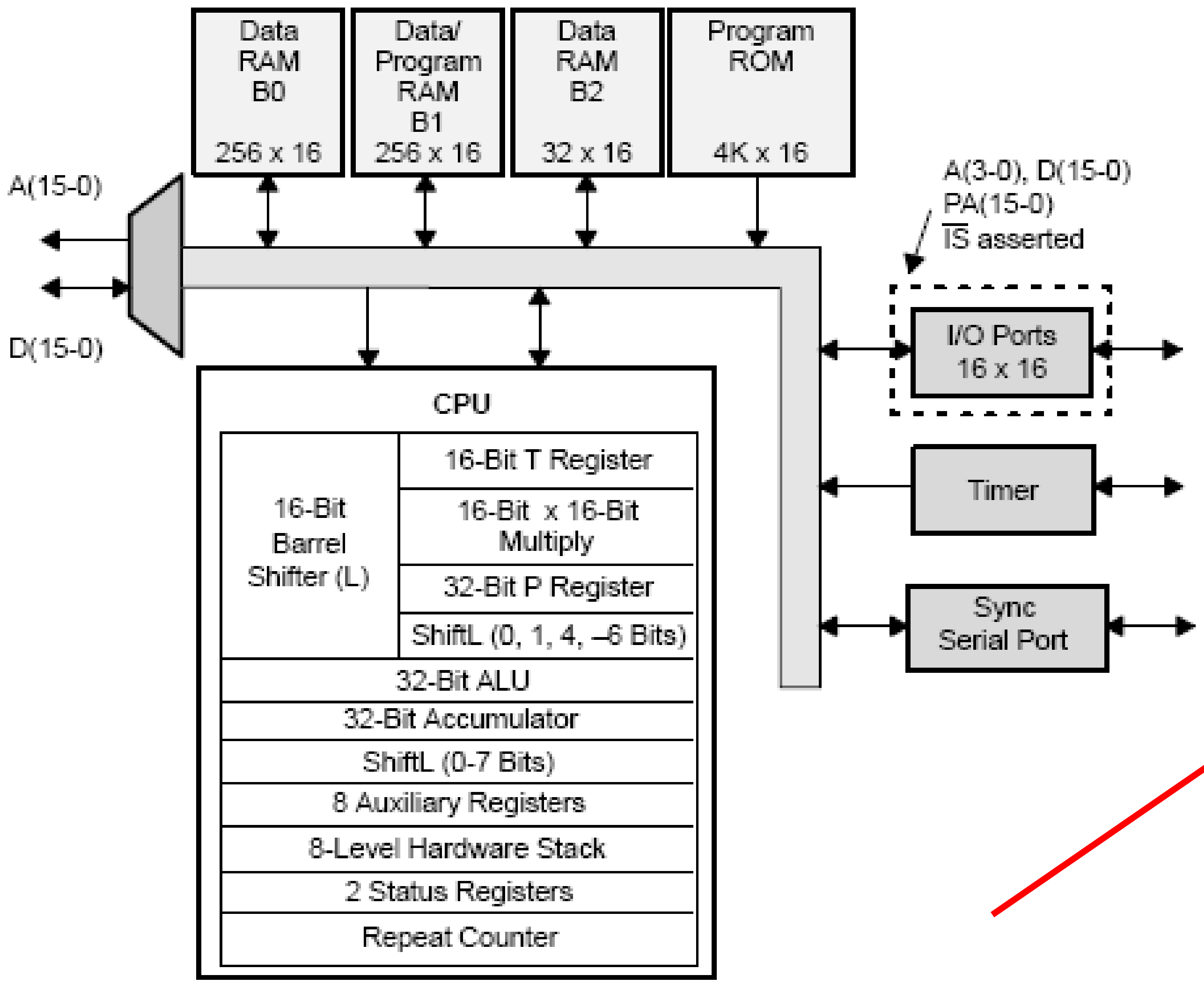
DX **(O/TS)** Serial data transmit output. Serial data transmitted from the XSR (serial port transmit shift register) via the DX pin. Placed in high-impedance state when not transmitting.

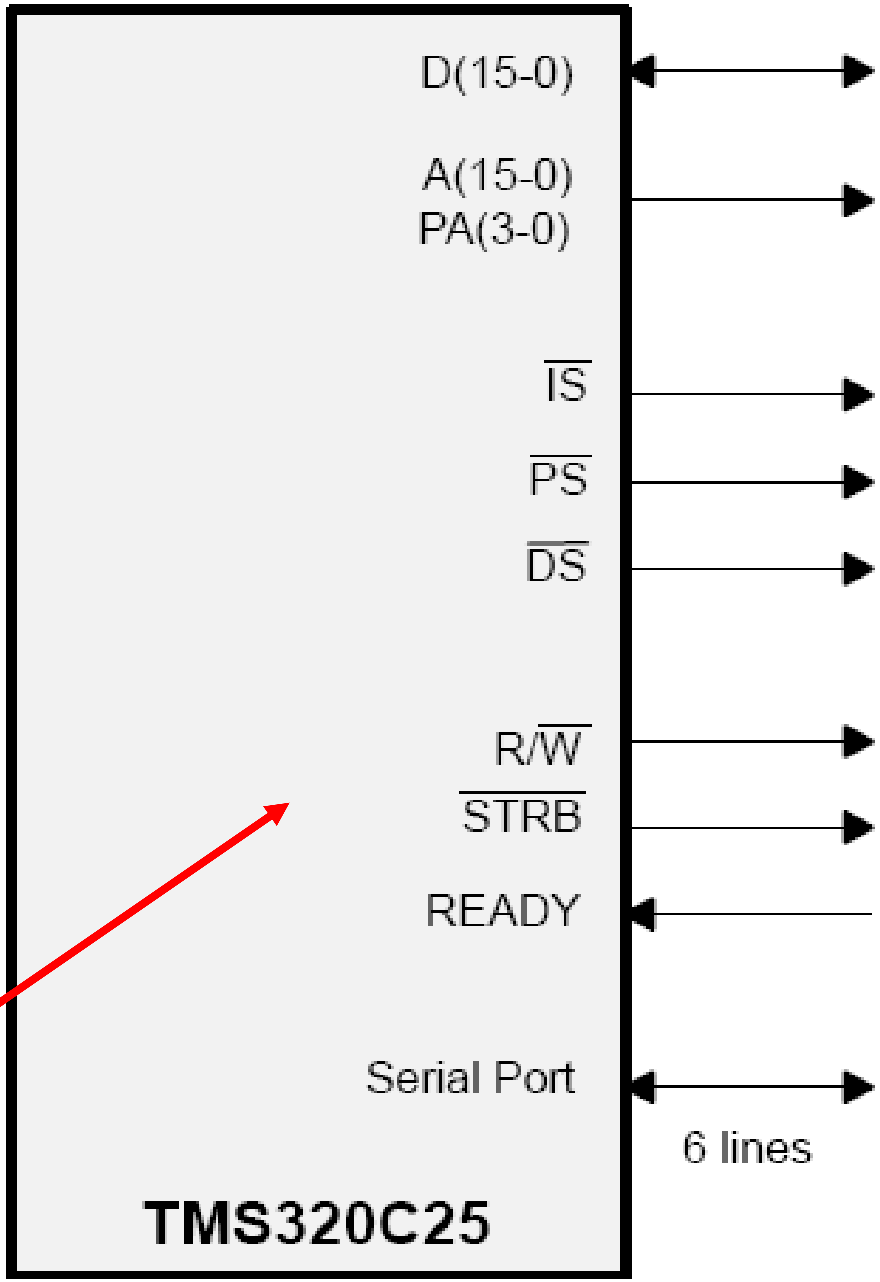
FSR **(I)** Frame synchronization pulse for receive input. The falling edge of the FSR pulse initiates the data-receive process, beginning the clocking of the RSR.

FSX **(I/O)** Frame synchronization pulse for transmit input/output. The falling edge of the FSX pulse initiates the data- transmit process, begin-ning the clocking of the XSR.Following reset, the default operat-ing condition of FSX is as an input. This pin may be selected by software to be an output when the TXM bit in the status register is set to 1.

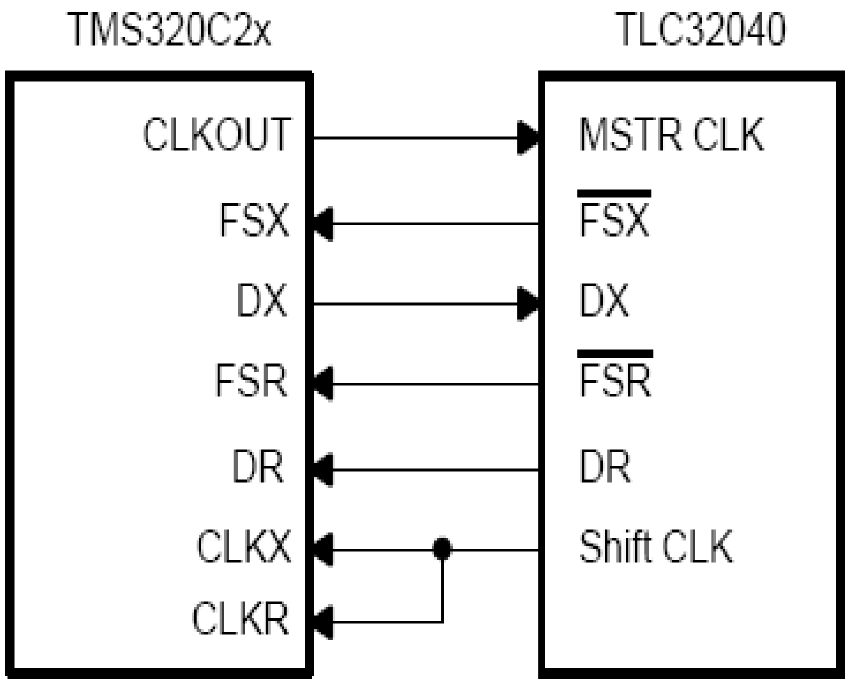
TMS320 Interface to Off-Chip Devices

TMS320C25 Block Diagram





Interface of TLC32040 to TMS320C2x



Synchronous Timing of TLC32040 to TMS320C2x